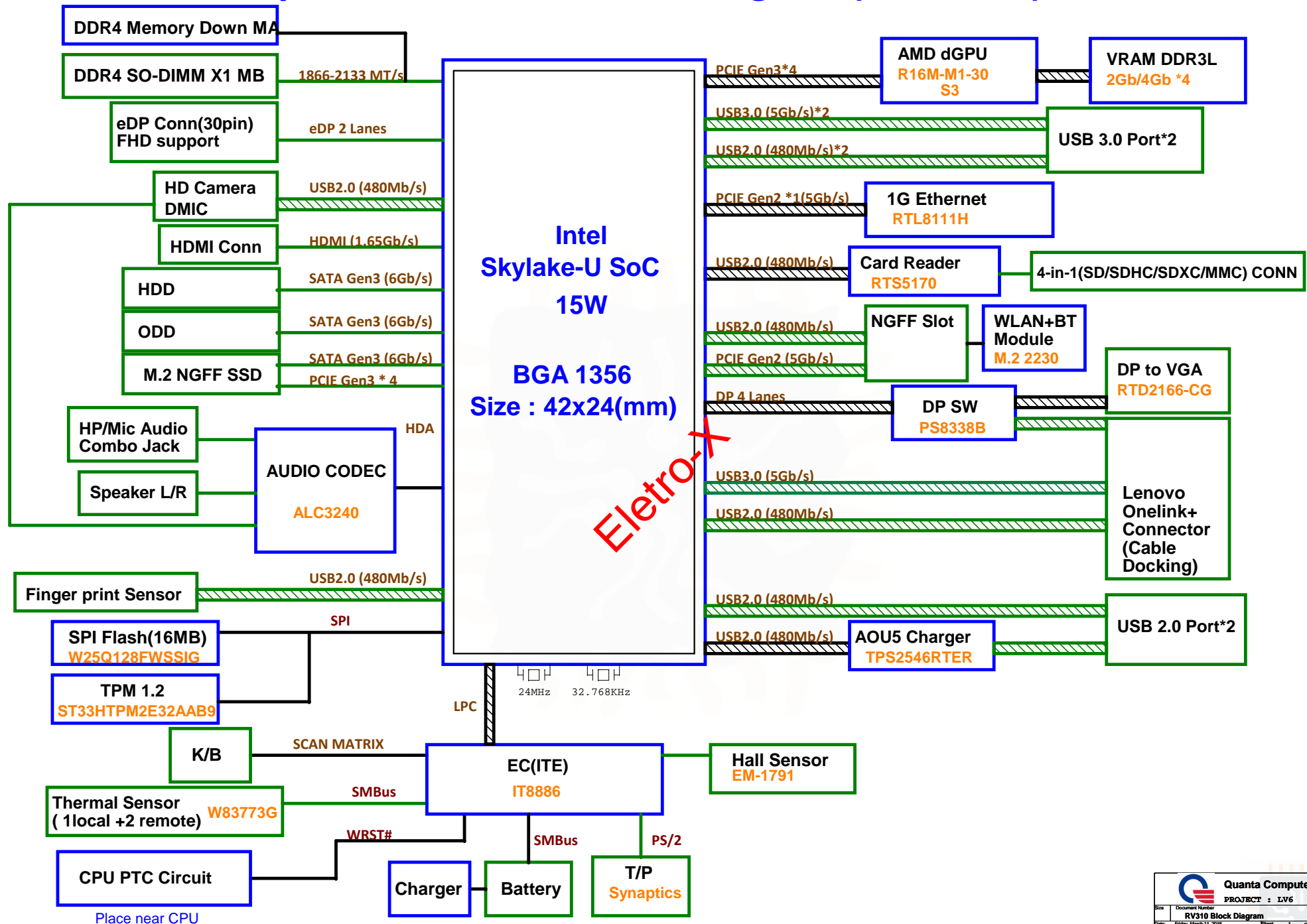
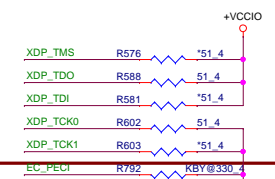
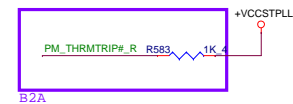
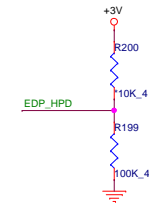


Intel Skylake-U Platform Block Diagram (Windows)

01



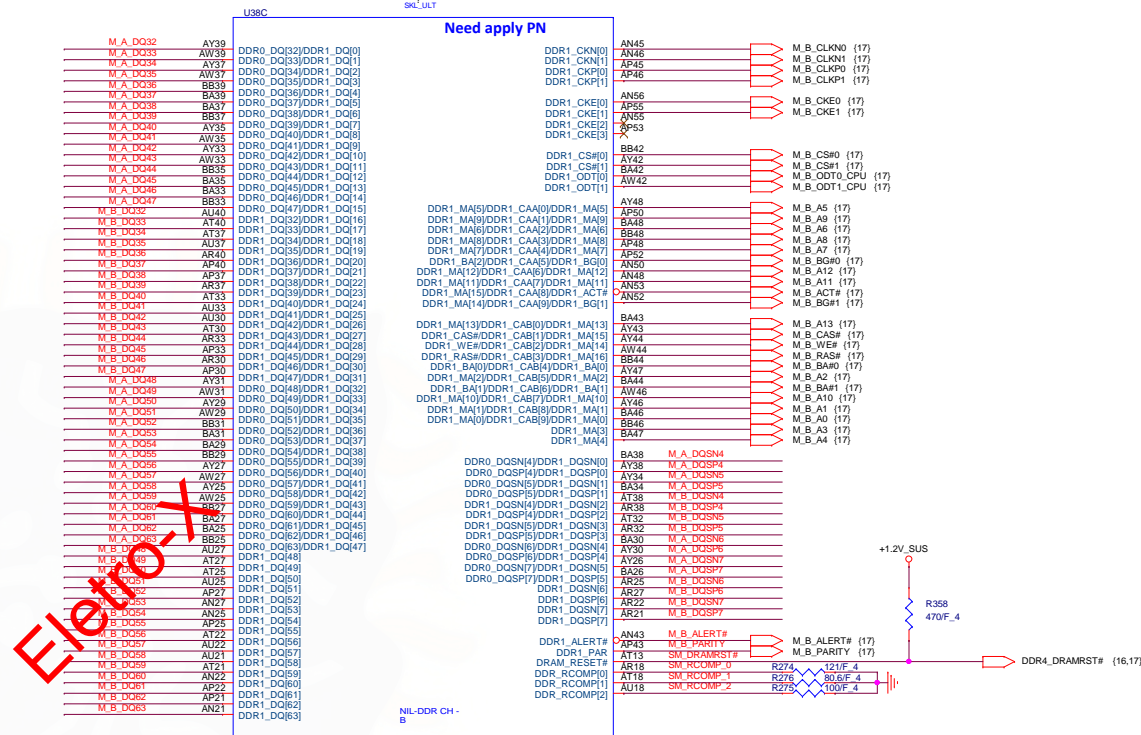
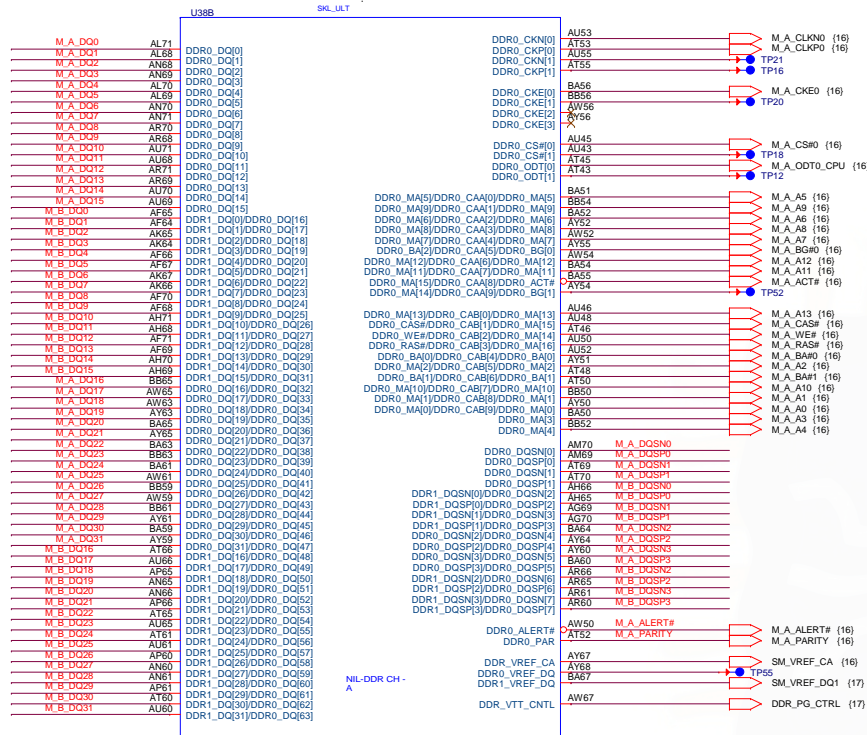



PLACE NEAR CPU



SkyLake ULT Processor (DDR4) Interleave

03





Quanta Computer Inc.
PROJECT : LV6

Size

Document Number

Rev 1A

SKYLAKE 2/15(DDR4 VF)

12/1F 4

30/6F 4

12/1F 4

30/6F 4

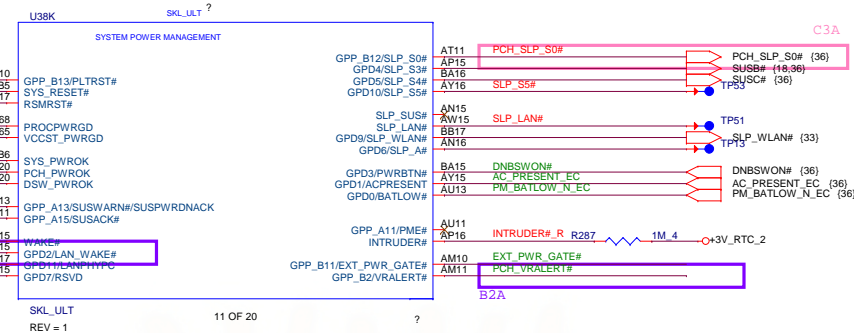
Date: Friday, March 11, 2016

Sheet 3 of 61

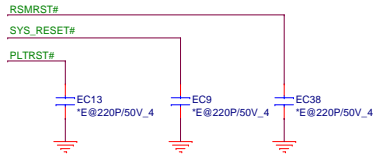
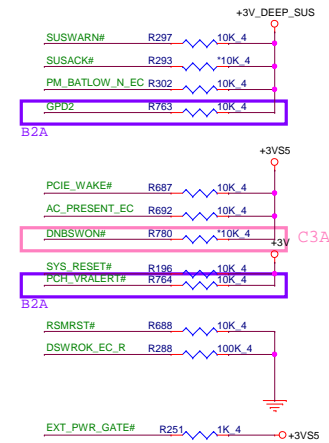
ELECTRO-0



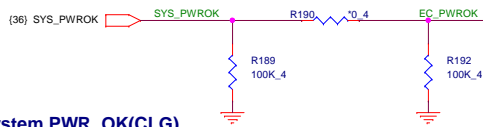
(10,11,14,15,17) +3V_DEEP_SUS
(2,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54)
(34,35,38,39,41,42,44,45,48,50,51,53,54,56)
(2,6,53,56) +VCCIO
(2,5,6,9,45,53,56) +VCCSTPLL
(13,15) +3V_RTC_2



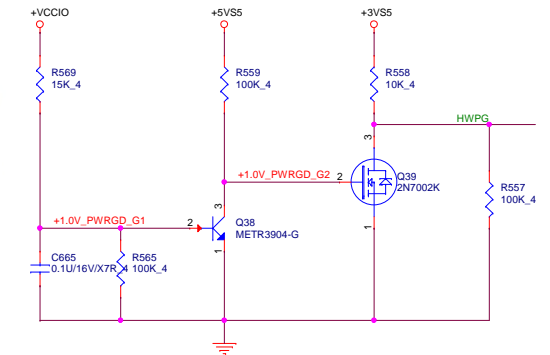
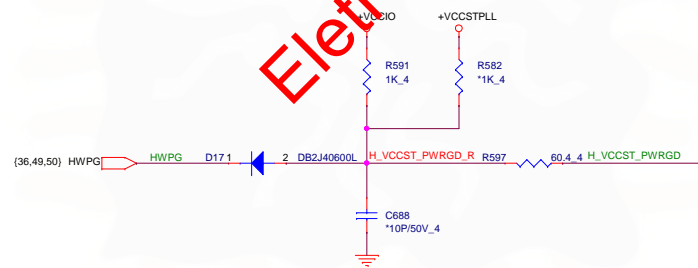
PCH Pull-high/low(CLG)



PLTRST#(CLG)



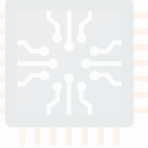
System PWR_OK(CLG)



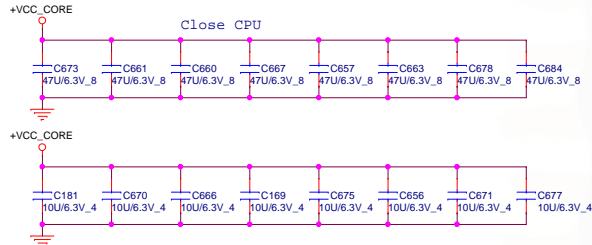
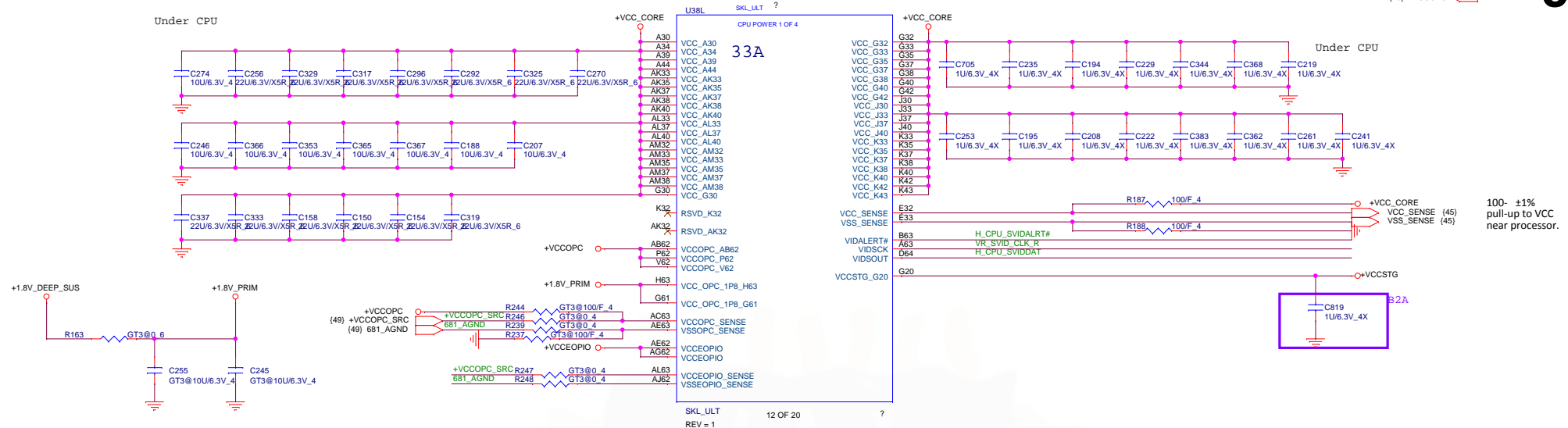
Quanta Computer Inc.

PROJECT : LV6

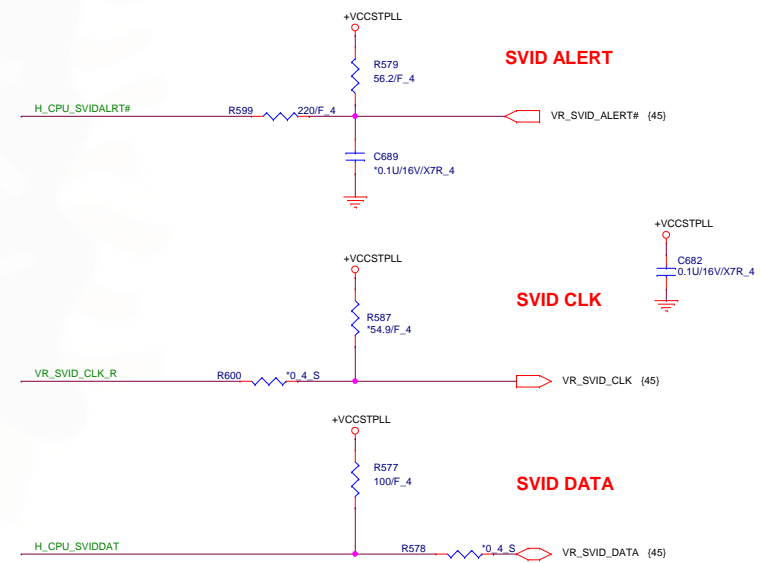
Size Document Number
SKYLAKE 3/15(PowerManger)
Date: Friday, March 11, 2016 Sheet 4 of 61 Rev 1A

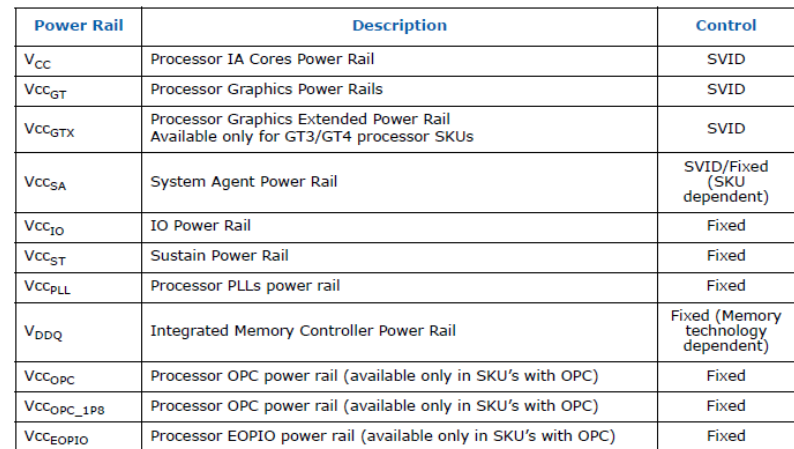


Under CPU

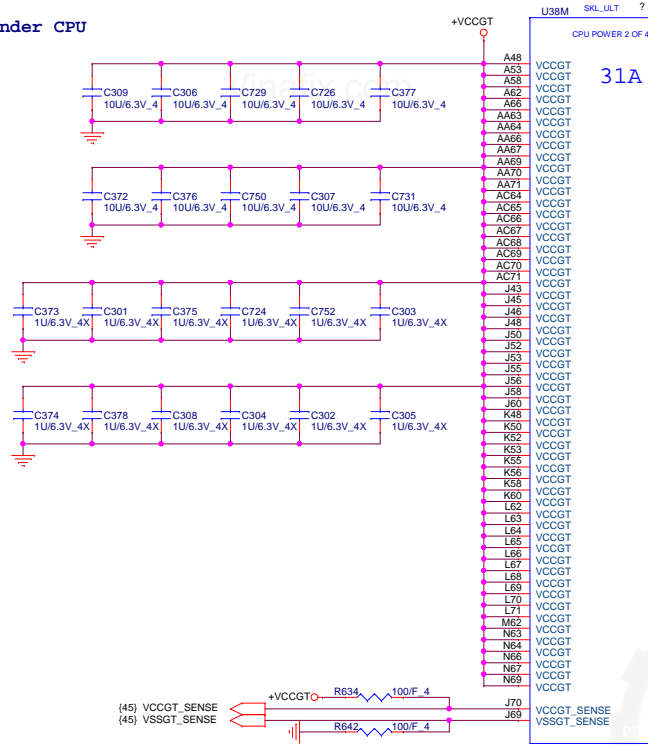


Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

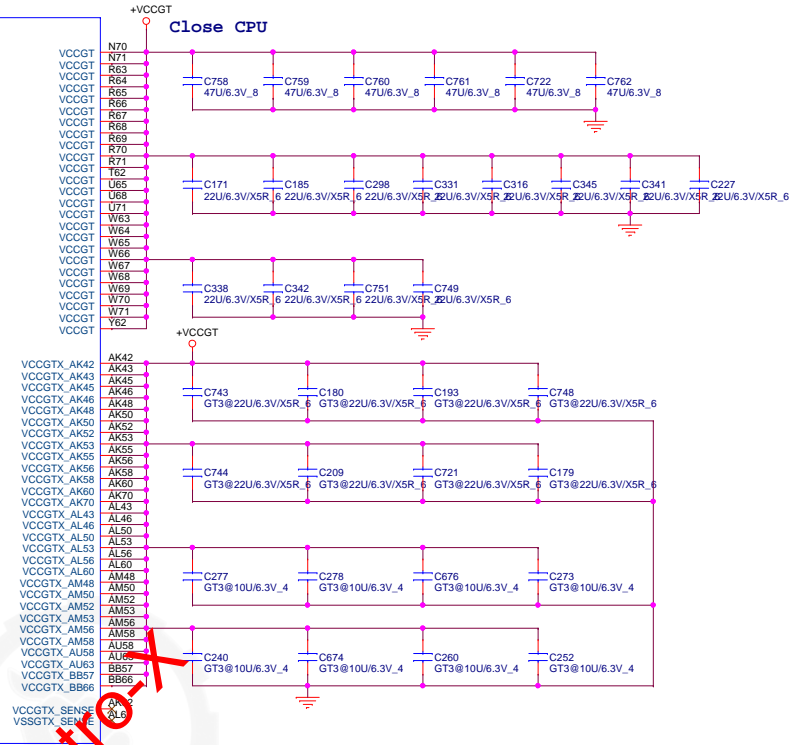




Under CPU



Close CPU



SKL_ULT 13 OF 20

REV = 1

Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1PB}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

+VCCGT (47)



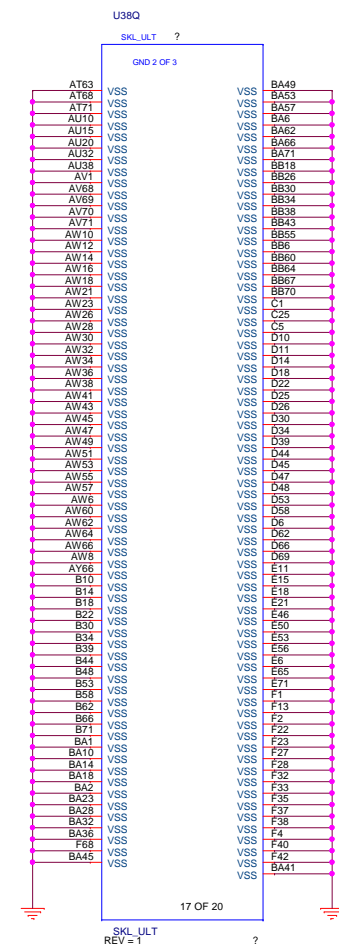
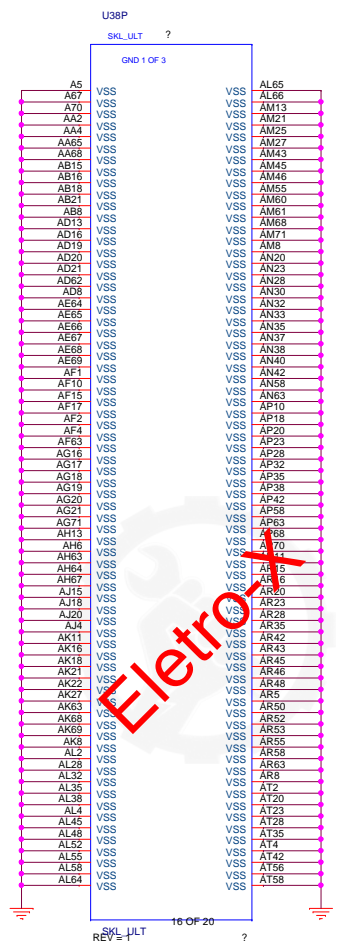
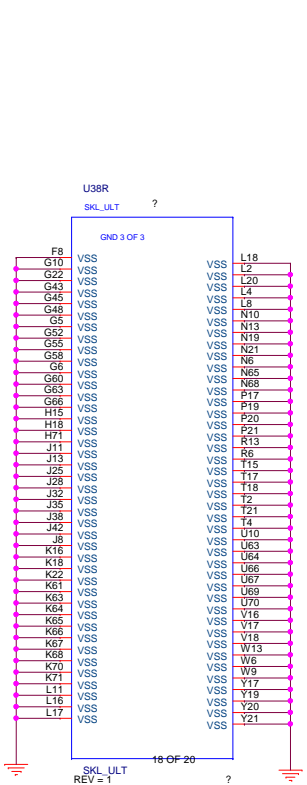
Quanta Computer Inc.

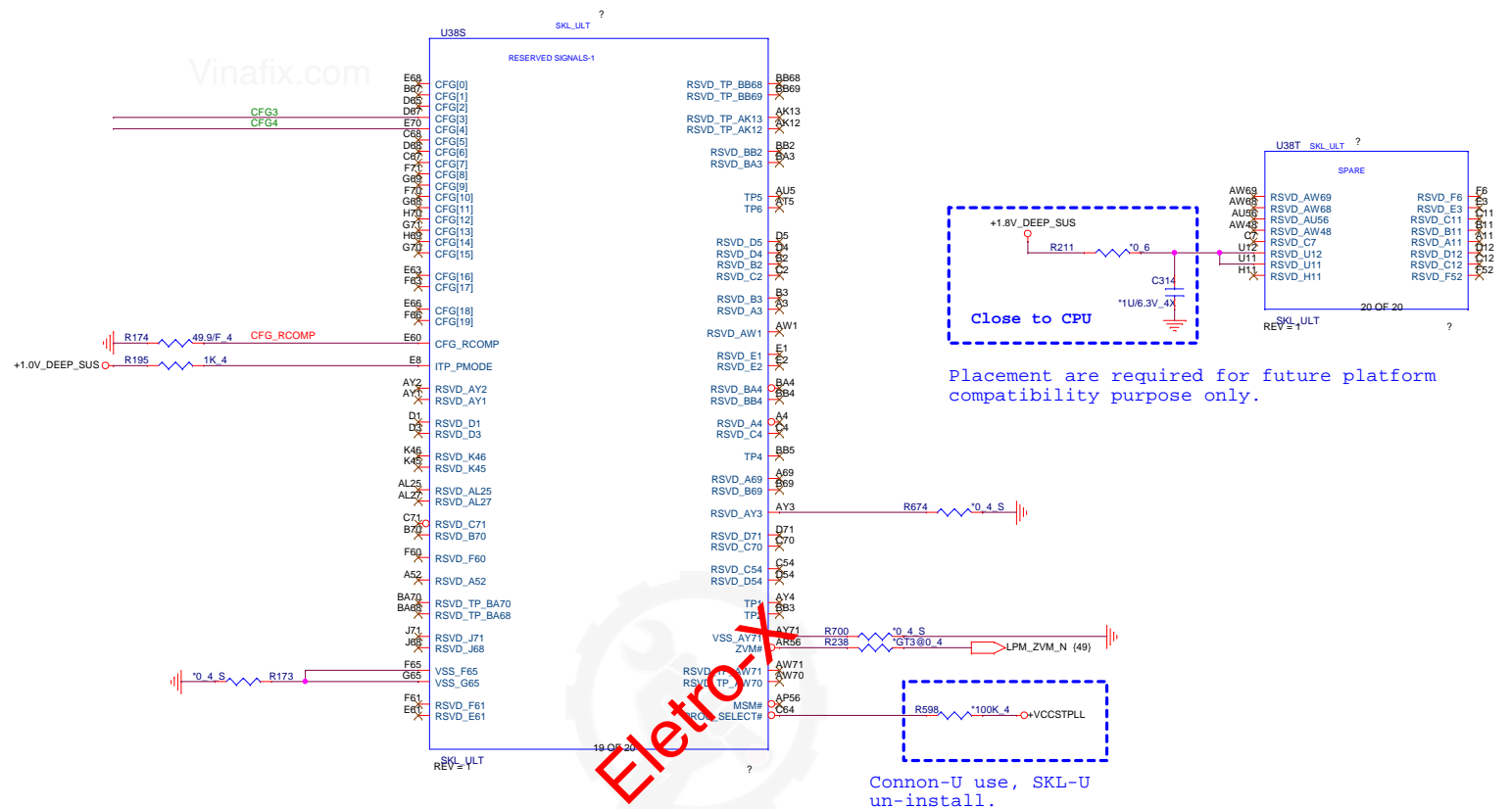
PROJECT : LV6

Size Document Number
SKYLAKE 6/15 (POWER-3)

Date: Friday, March 11, 2016 Sheet 7 of 61

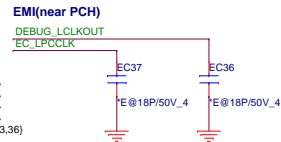
Rev 1A






Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX_Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R611 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R617 *1K_4



TP70	●	←	PCH_SPI_CS0#_R	→	PCH_SPI_CS0#_R (36)
TP67	●	←	PCH_SPI1_CLK_R	→	PCH_SPI1_CLK_R (36)
TP68	●	←	PCH_SPI1_SI_R	→	PCH_SPI1_SI_R (36)
TP69	●	←	PCH_SPI1_SO_R	→	PCH_SPI1_SO_R (36)
TP22	●	←	BIOS_WP#		
TP23	●	←	HOLD#		

[illegible]

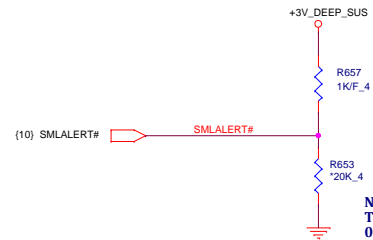
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Size	Document Number	Rev
	SKYLAKE 9/15(SPI/LPC/SM)	1A
Date:	Friday, March 11, 2016	Sheet 10 of 61

Functional Strap Definitions

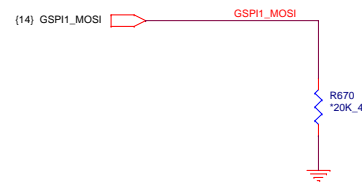
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



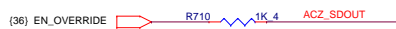
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.
Bit 10 Boot BIOS Destination
0 SPI
1 LPC



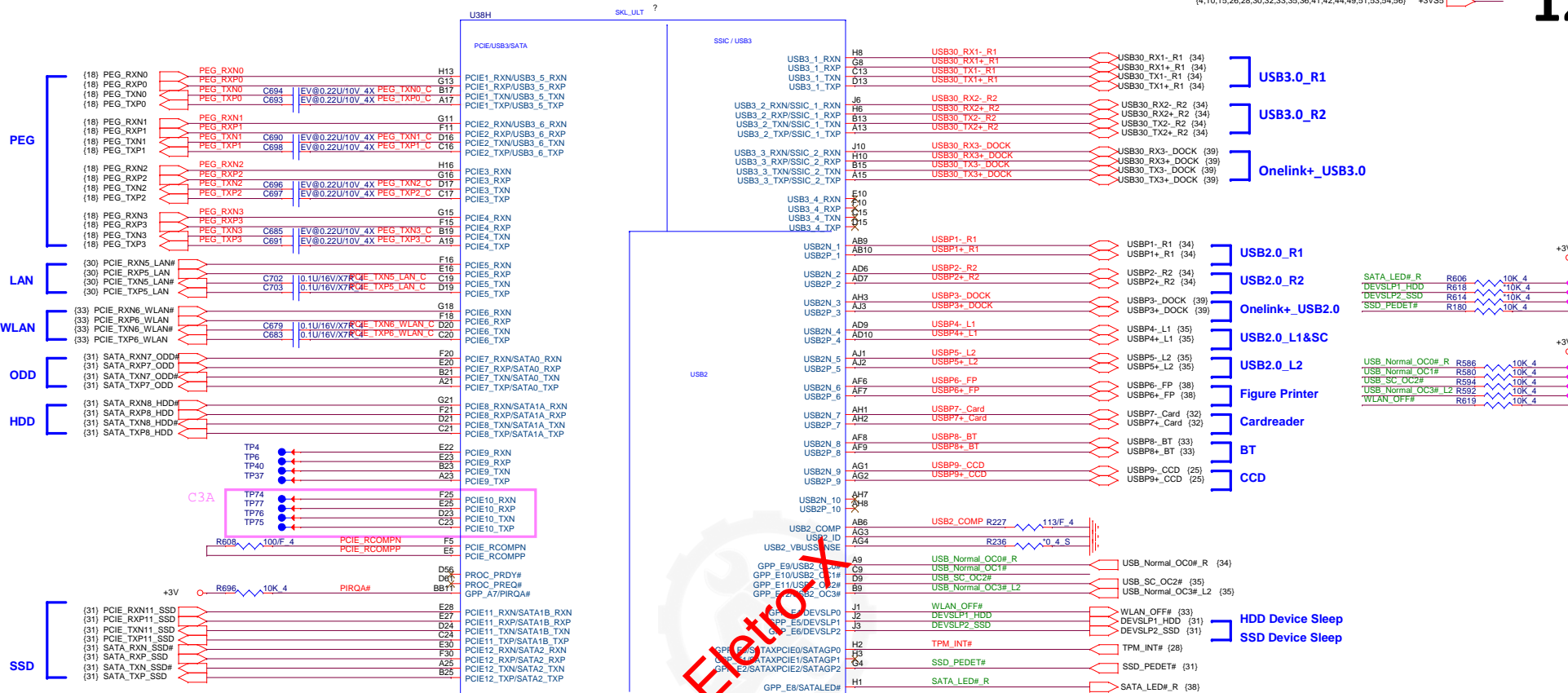
No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
0 = LPC is selected for EC.
1 = eSPI is selected for EC.



PCI-E Port Mapping Table

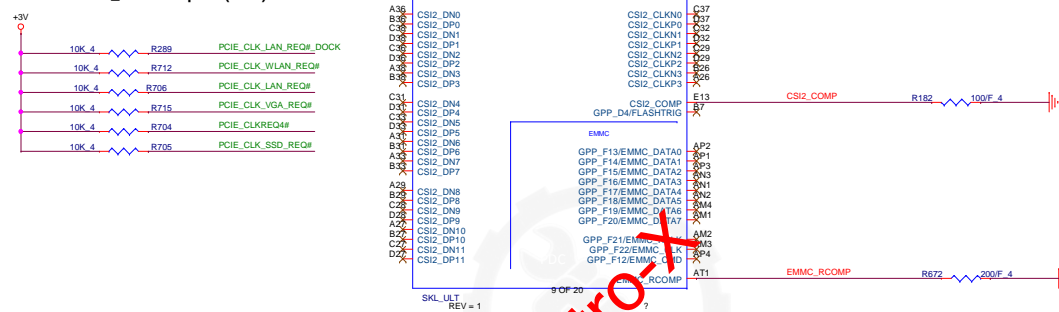
PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	dGPU
Port2		Port1	LAN
Port3		Port2	WLAN
Port4		Port3	DOCK
Port5	LAN	Port4	Un-used
Port6	WLAN	Port5	SSD
Port7	ODD		
Port8	HDD		
Port9	Un-used		
Port10	DOCK		
Port11	SSD		
Port12			

USB3.0 Port Mapping Table

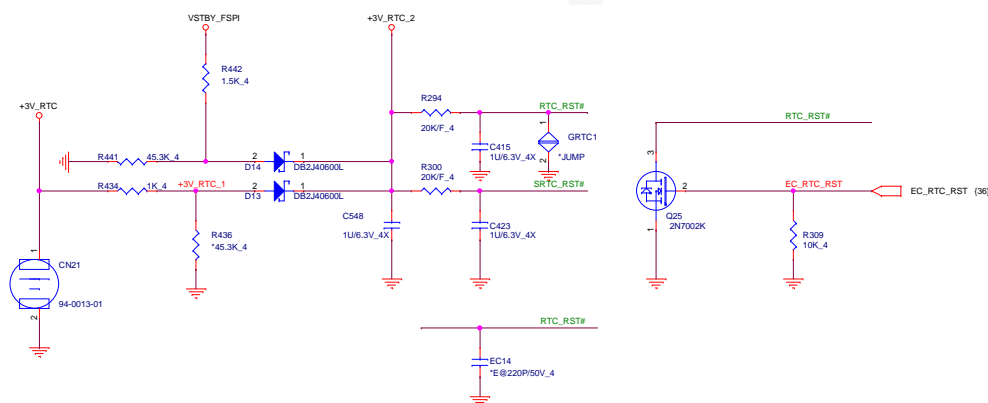
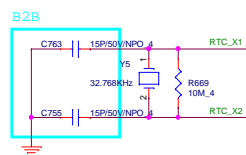
USB3.0	Function
PORT-1	USB3.0_R1
PORT-2	USB3.0_R2
PORT-3	USB3.0_DOCK
PORT-4	

USB2.0 Port Mapping Table

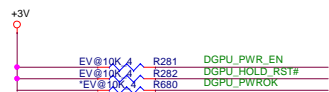
USB2.0	Function
PORT-1	USB2.0_R1
PORT-2	USB2.0_R2
PORT-3	USB2.0_DOCK
PORT-4	USB2.0_L1_S&C
PORT-5	USB2.0_L2
PORT-6	Figure Printer
PORT-7	Cardreader
PORT-8	BT
PORT-9	CCD
PORT-10	NC



RTC Power trace width 20mils.



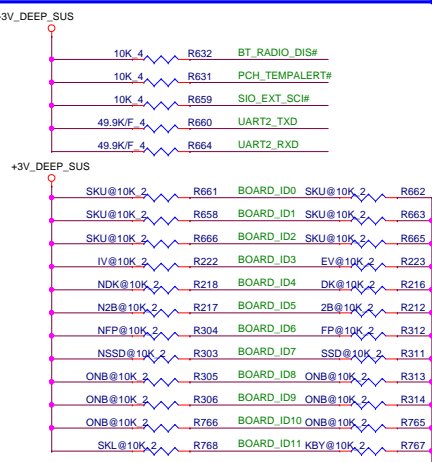
DGPU <VGA>



<CPU>

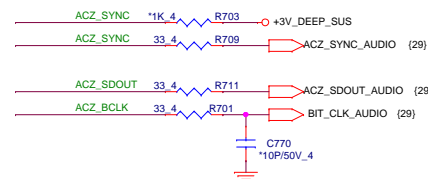
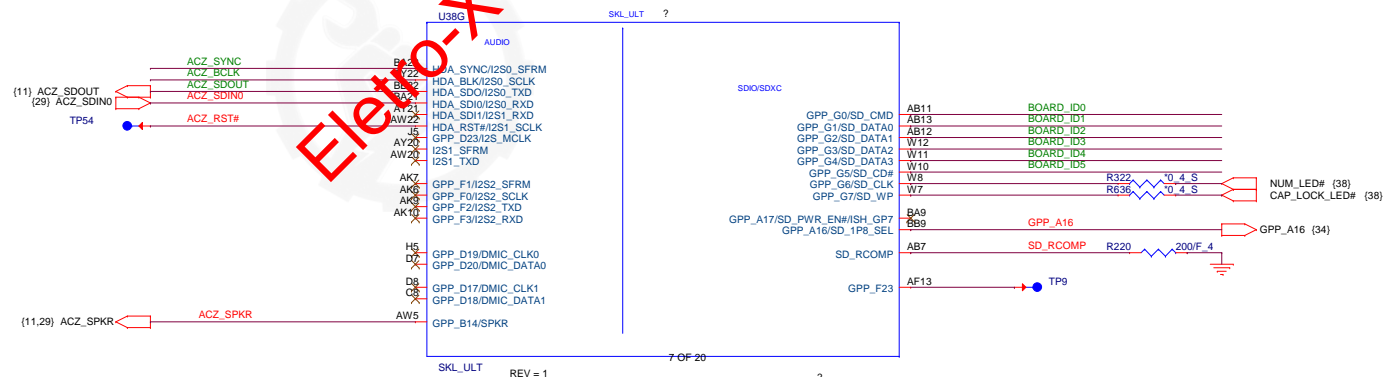
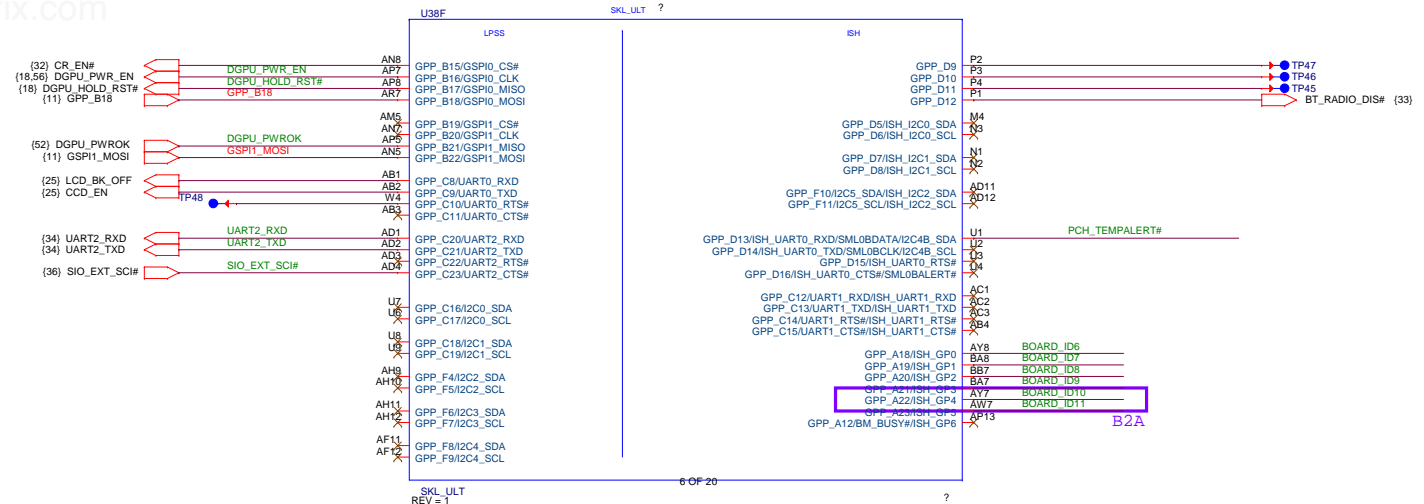
Vinafix.com

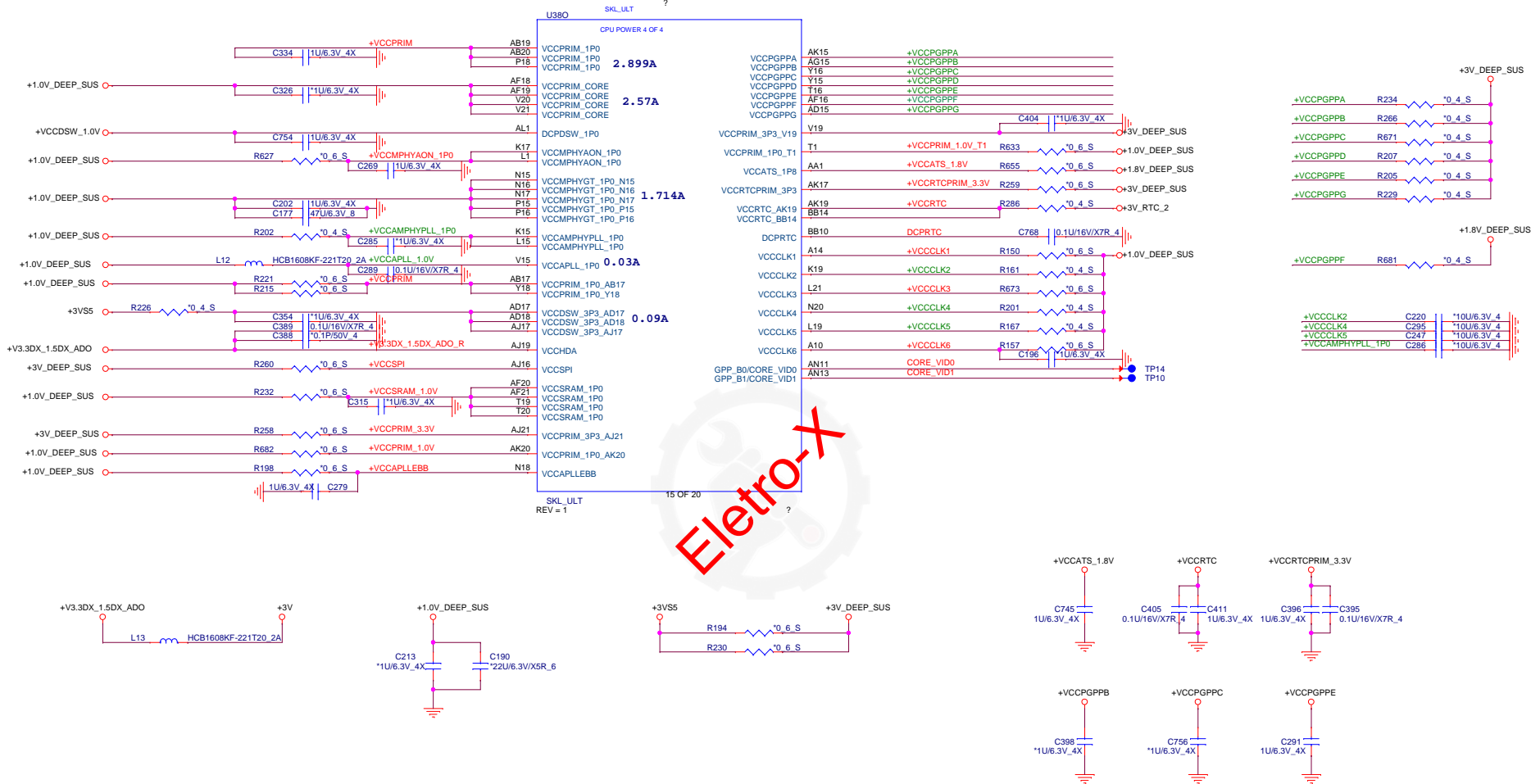
Skylake (GPIO)



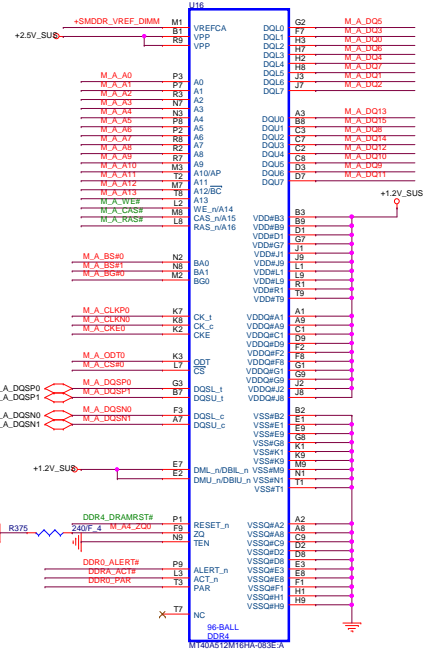
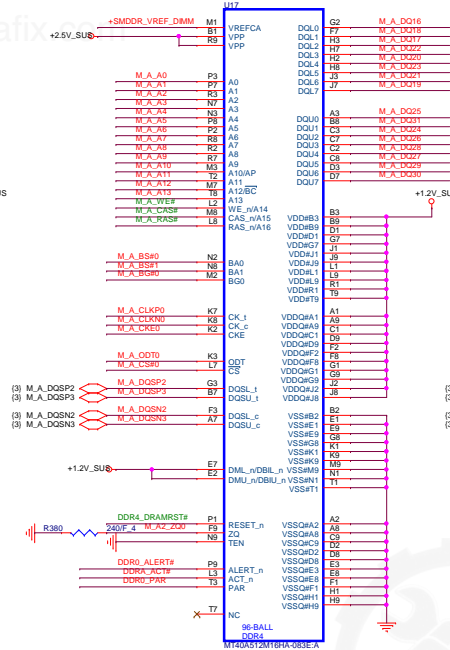
Sku	Model	BOARD_ID0	BOARD_ID1	BOARD_ID2
0	E42(R310_14)	0	0	0
1	E52(R310_15)	0	0	1
2	V310_14	0	1	0
3	V310_15	0	1	1
4	Tiany310_14	1	0	0
5	Tiany310_15	1	0	1
6	Reserved	1	1	0
7	Reserved	1	1	1

BOARD_ID3	Hi = UMA	Lo = Discrete
BOARD_ID4	Hi = wo Prolink	Lo = w Prolink
BOARD_ID5	Hi = wo 2nd Battery	Lo = w 2nd Battery
BOARD_ID6	Hi = wo Figure Printer	Lo = w Figure Printer
BOARD_ID7	Hi = wo SSD	Lo = w SSD
On Board Memory	[1, 1, 1] = Samsung K4A8G165WB-BCRC [1, 1, 0] = Micro MT40A512M16JY-083E:B [1, 0, 1] = SMART	D3A B2A
BOARD_ID8	[1, 0, 0] = Teikou [0, 1, 1] = Samsung K4A8G165WB-BCPB [0, 1, 0] = Micro MT40A512M16HA-083E:A [0, 0, 1] = Hynix H5AN6G6NAFR-TFC	C3A
BOARD_ID11	[0, 0, 0] = No Memory Down Hi = Skylake Lo = Kaby lake	B2A

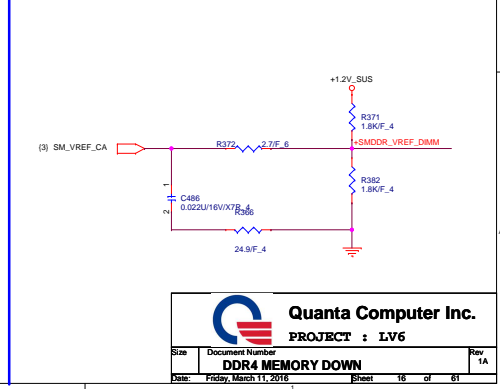
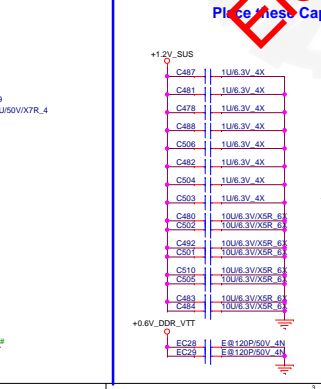


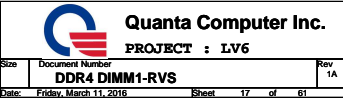


BYTE2_16-23
BYTE3_24-31

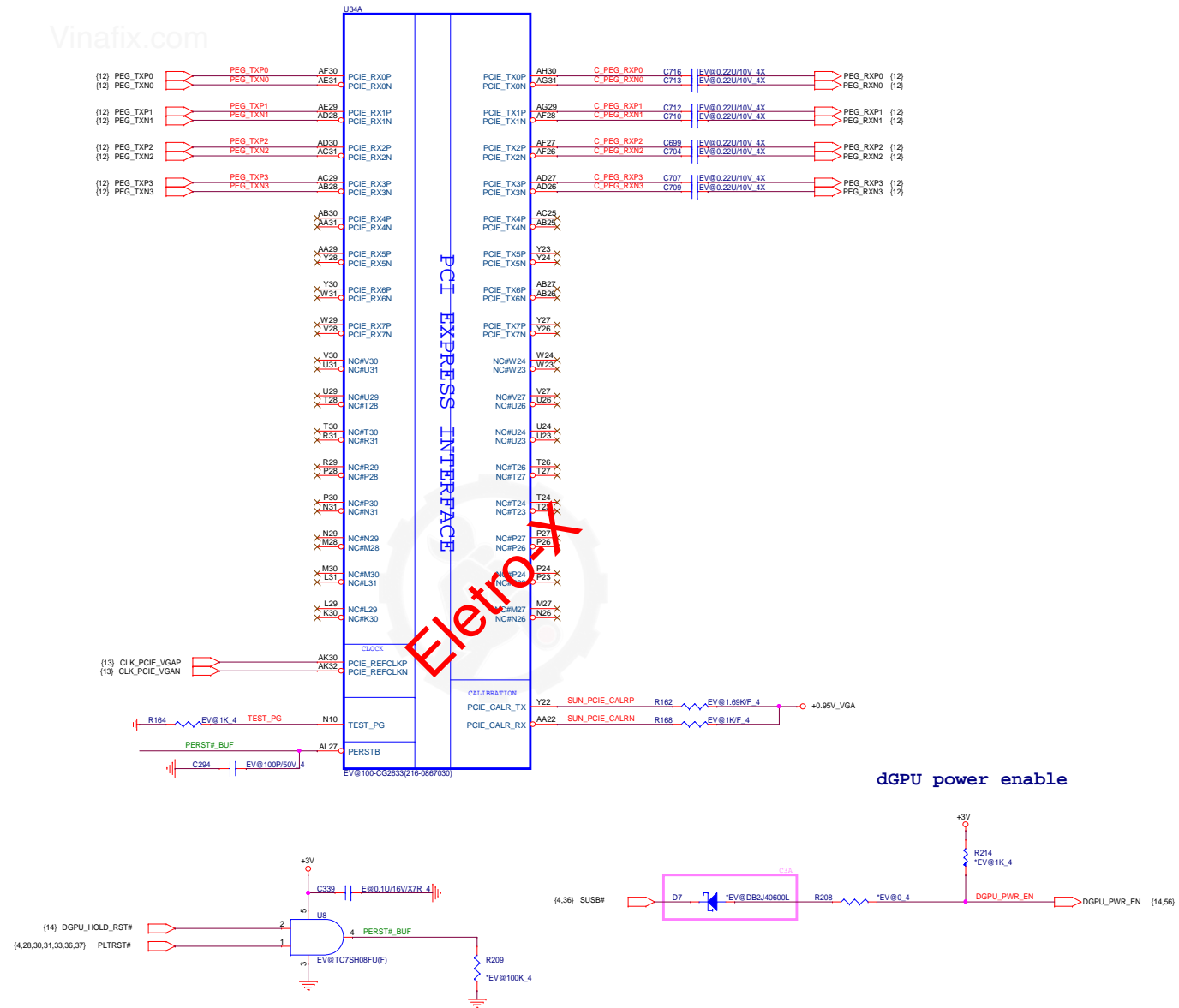


Place these Caps near Channel A

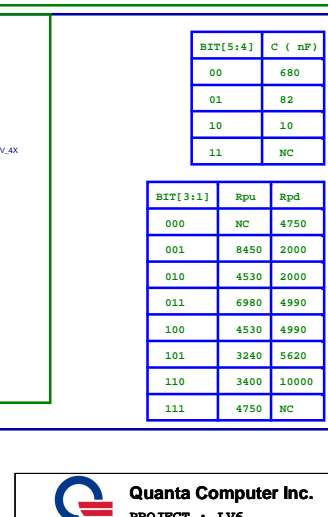
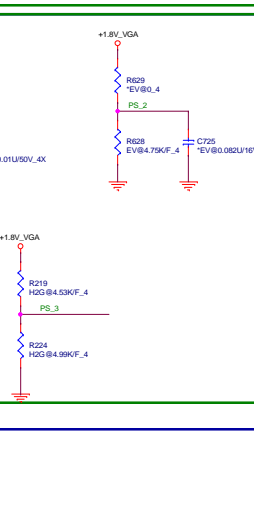
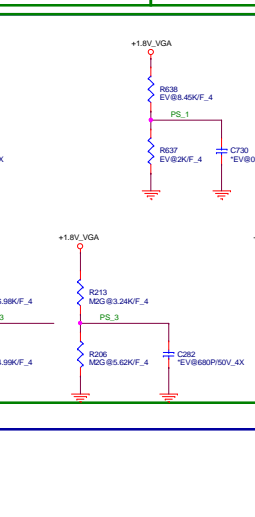
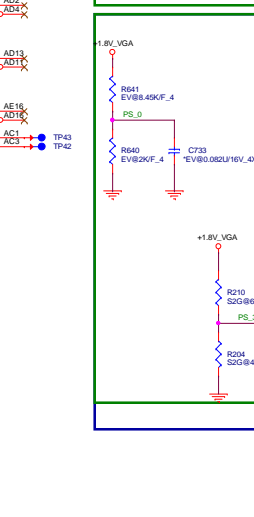
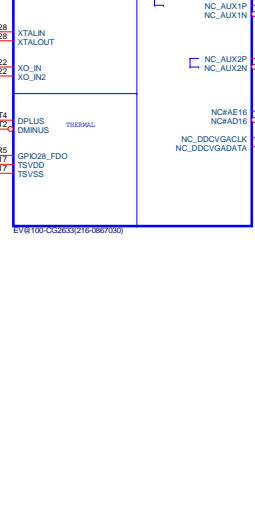
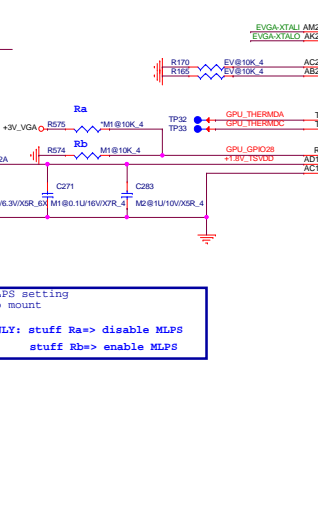
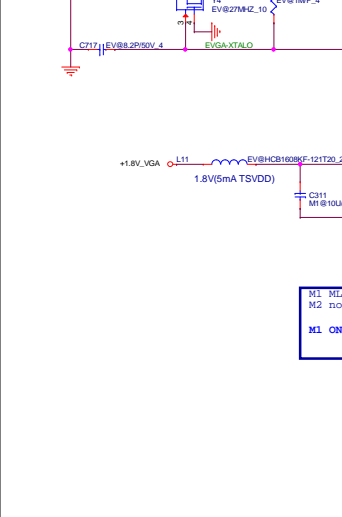
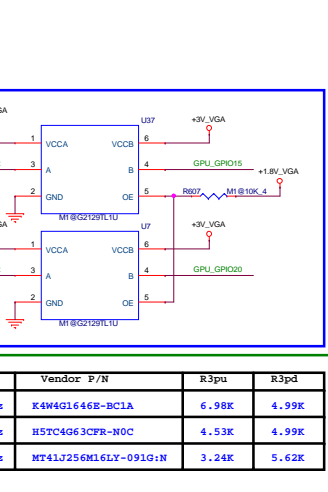
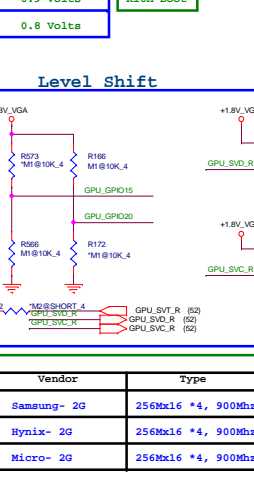
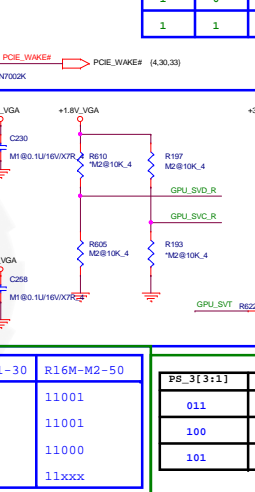
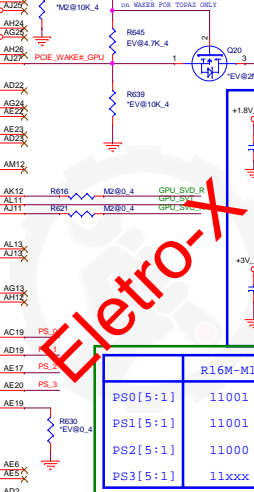
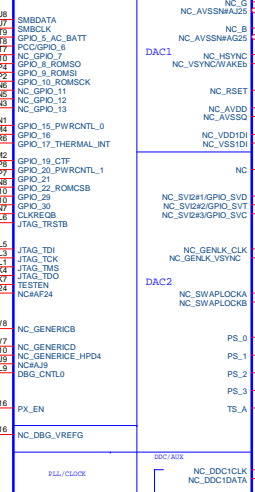
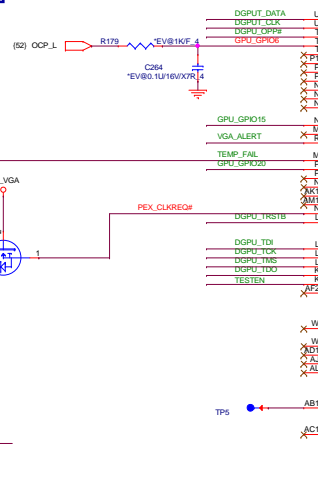
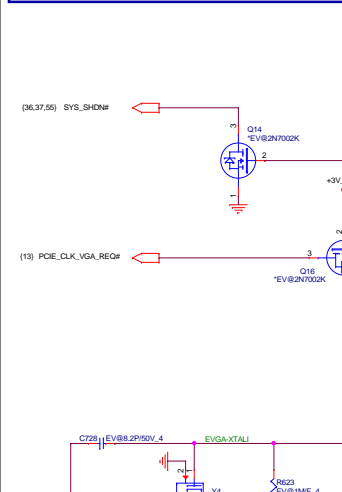
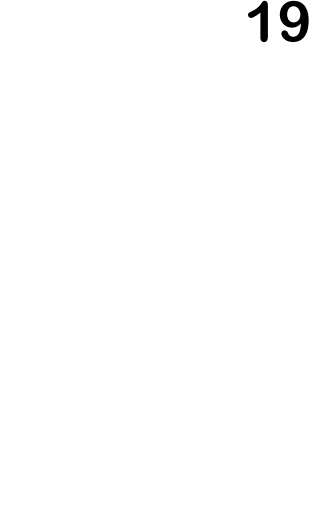
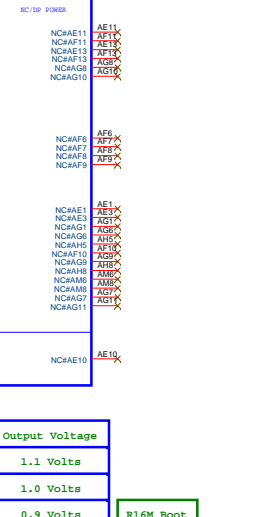
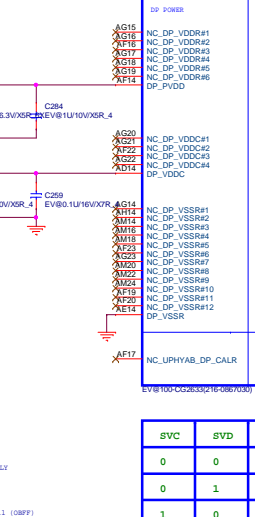
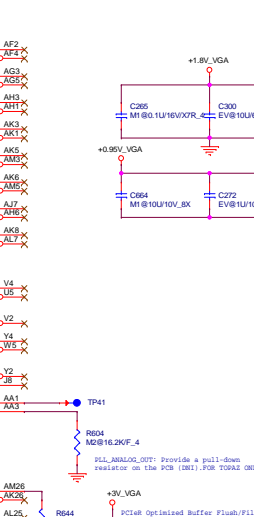
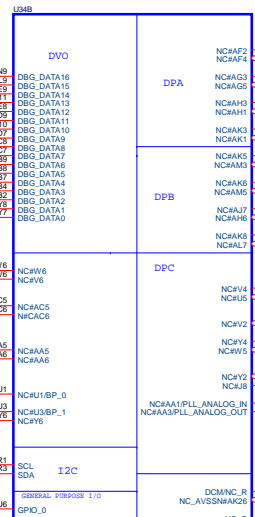
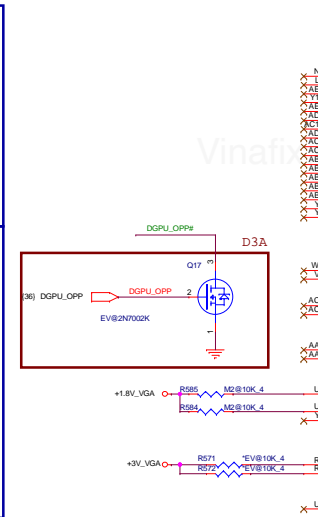
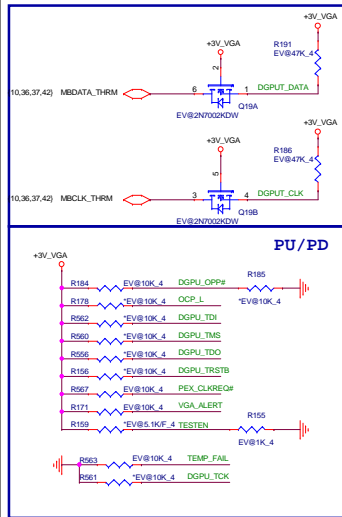




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dGPU power enable



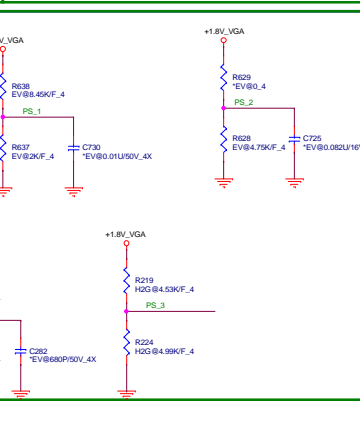
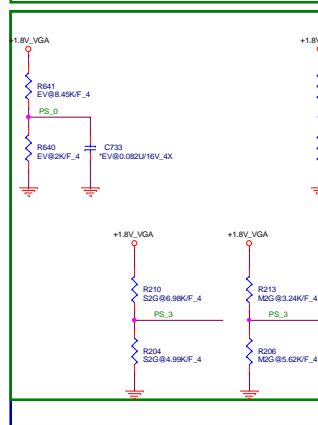
SVC	SVD	Output Voltage
0	0	1.1 Volts
0	1	1.0 Volts
1	0	0.9 Volts
1	1	0.8 Volts

R16M Boot

Eleto-X

	R16M-M1-30	R16M-M2-50
PS0[5:1]	11001	11001
PS1[5:1]	11001	11001
PS2[5:1]	11000	11000
PS3[5:1]	11xxxx	11xxxx

PS_3[3:1]	Vendor	Type	Vendor P/N	R3pu	R3pd
011	Samsung- 2G	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	6.98K	4.99K
100	Hynix- 2G	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	4.53K	4.99K
101	Micro- 2G	256Mx16 *4, 900Mhz	MT41J256M16LY-091G:N	3.24K	5.62K

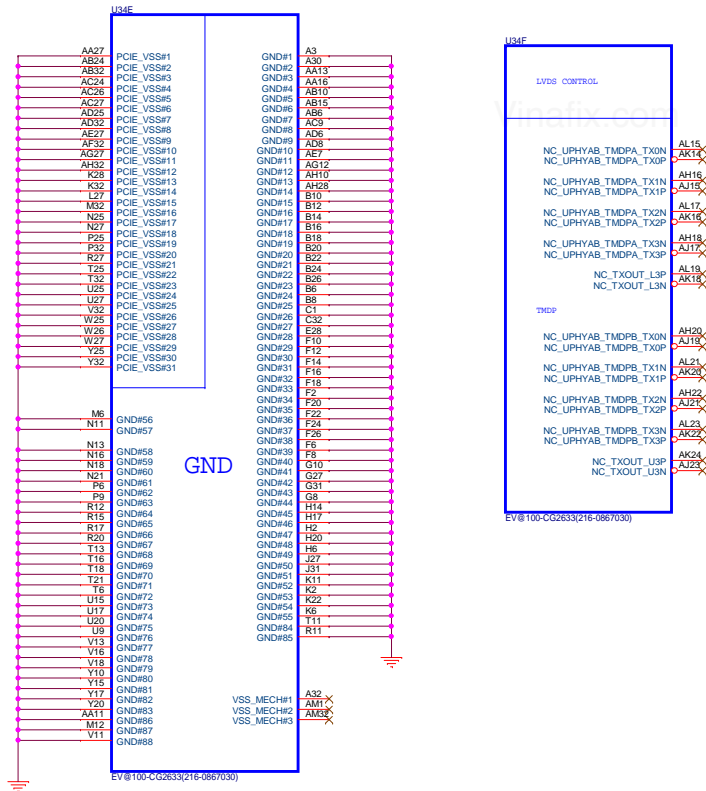


BIT[5:4]	C (nF)
00	680
01	82
10	10
11	NC

BIT[3:1]	Rpu	Rpd
000	NC	2700
001	8450	4050
010	4530	2000
011	6980	4990
100	4530	4990
101	3240	5620
110	3400	10000
111	4750	NC

M1 MLPS setting
M2 no mount

M1 ONLY: stuff Rb=> disable MLPS
stuff Rb=> enable MLPS

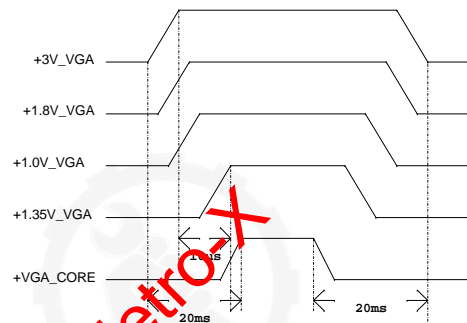


All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ps.

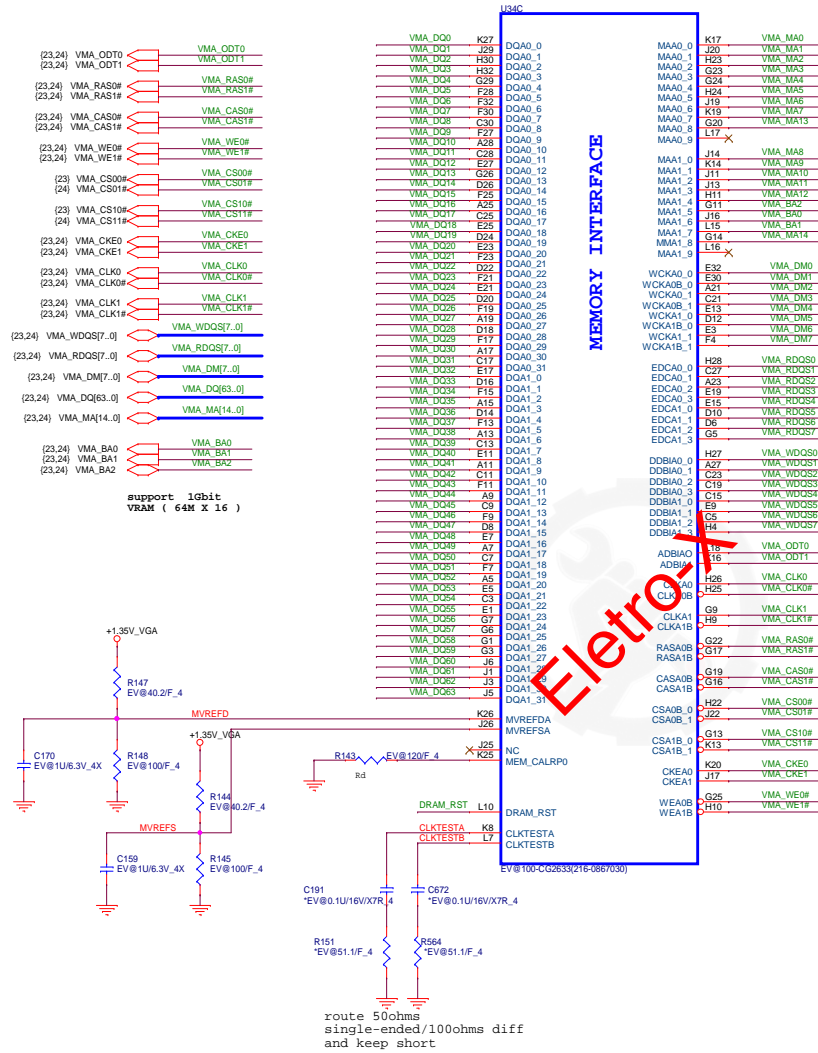
It is recommended that the 3.3-V rail ramp up first. The 3.3-V, 1.8-V, and 1.0-V rails must reach their ready state at least 10 μ s before VDDC, VDDCI, and VMEMIO start to ramp up.

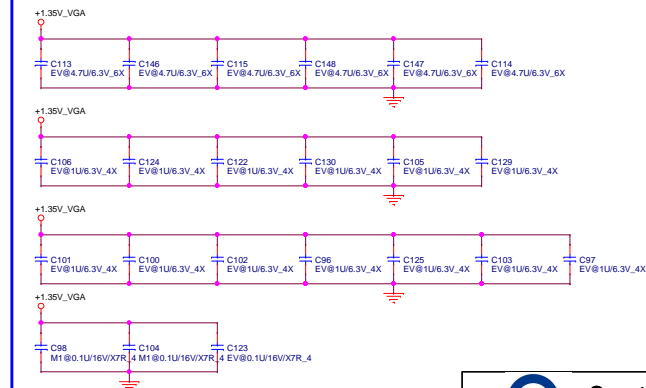
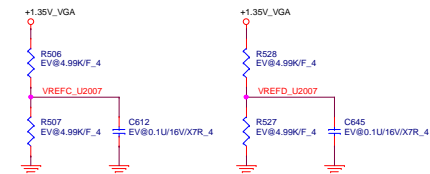
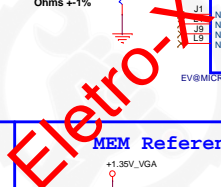
For power down, reversing the ramp-up sequence is recommended.

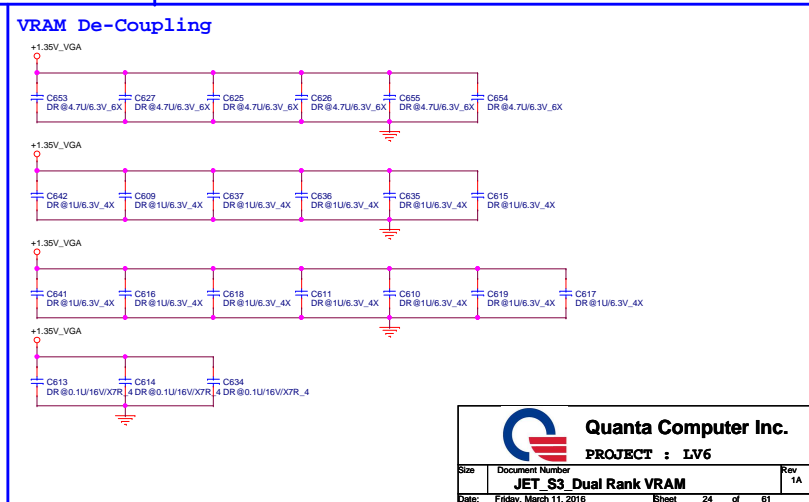
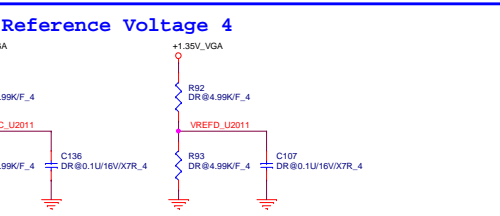
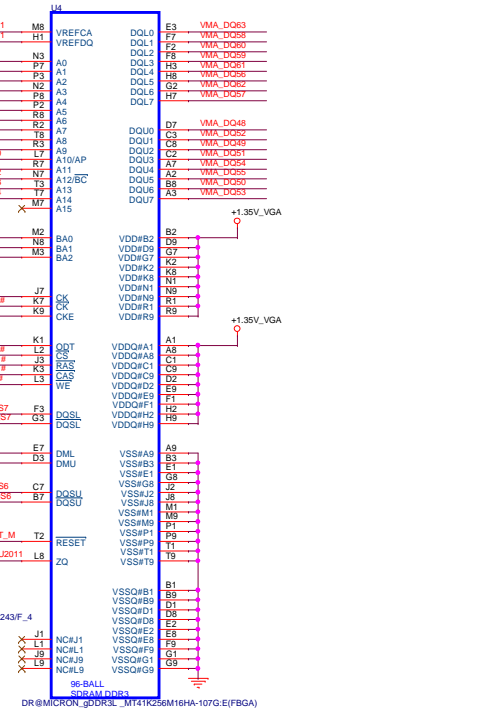
Power Up/Down Sequence

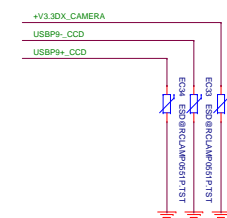
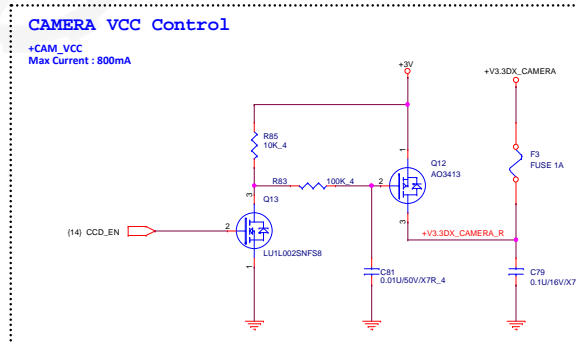
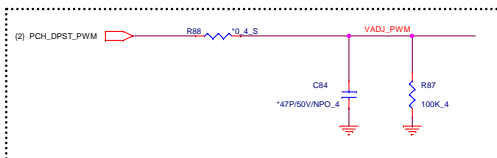
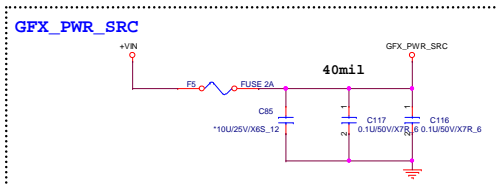
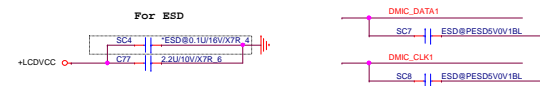
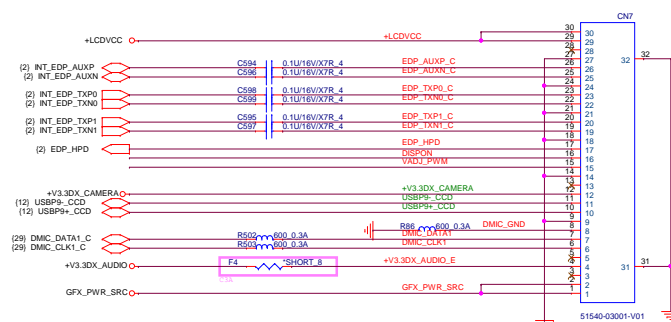
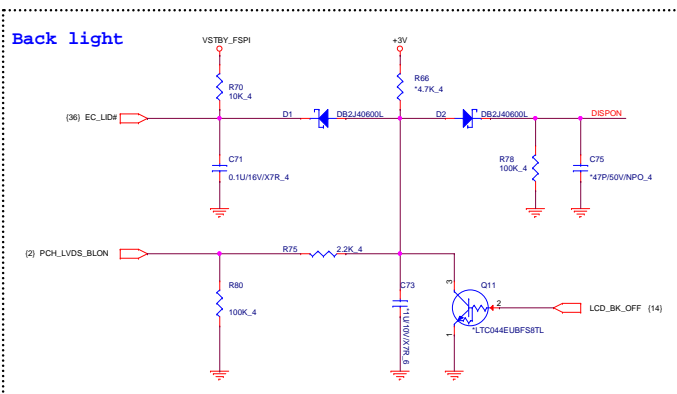
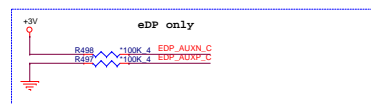
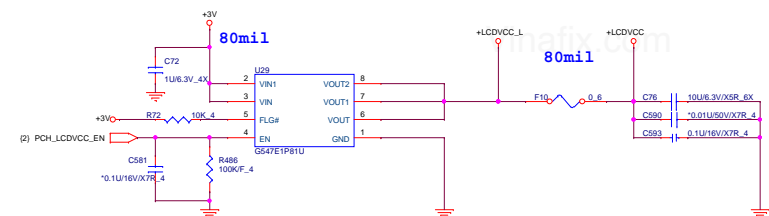




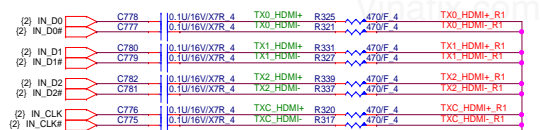




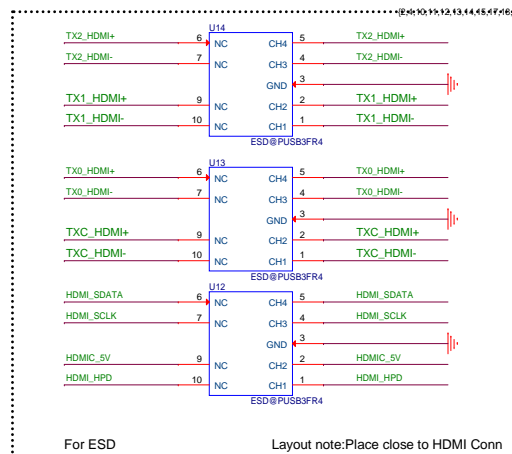
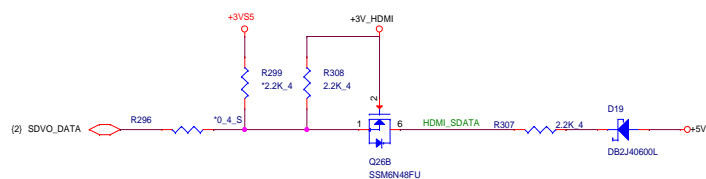
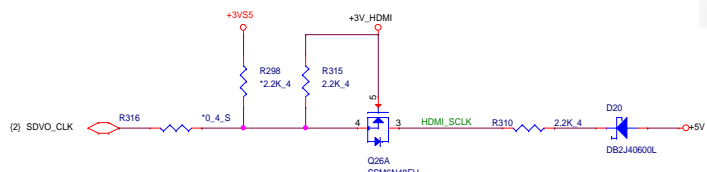
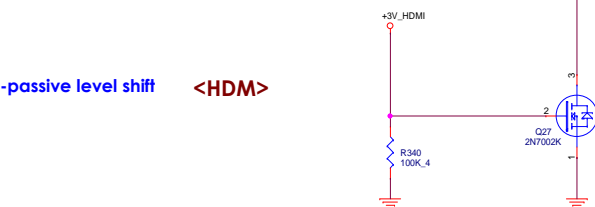




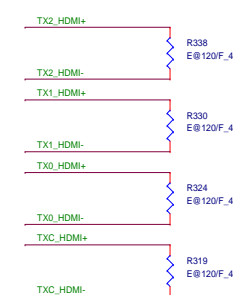
HDMI Conn <HDM>



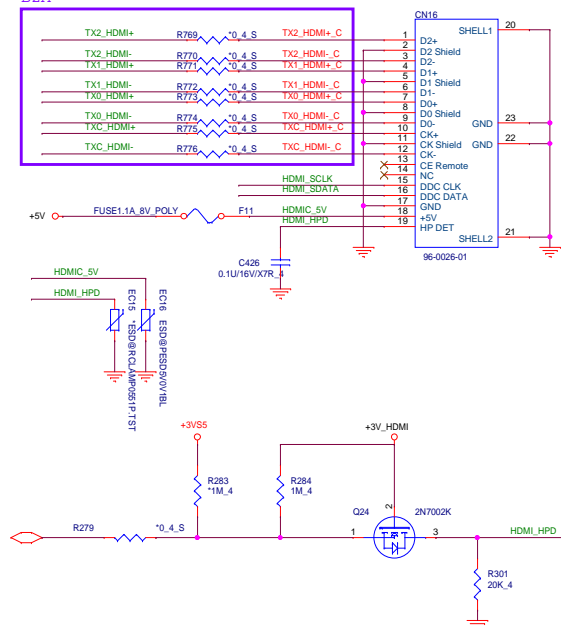
HDMI-passive level shift <HDM>

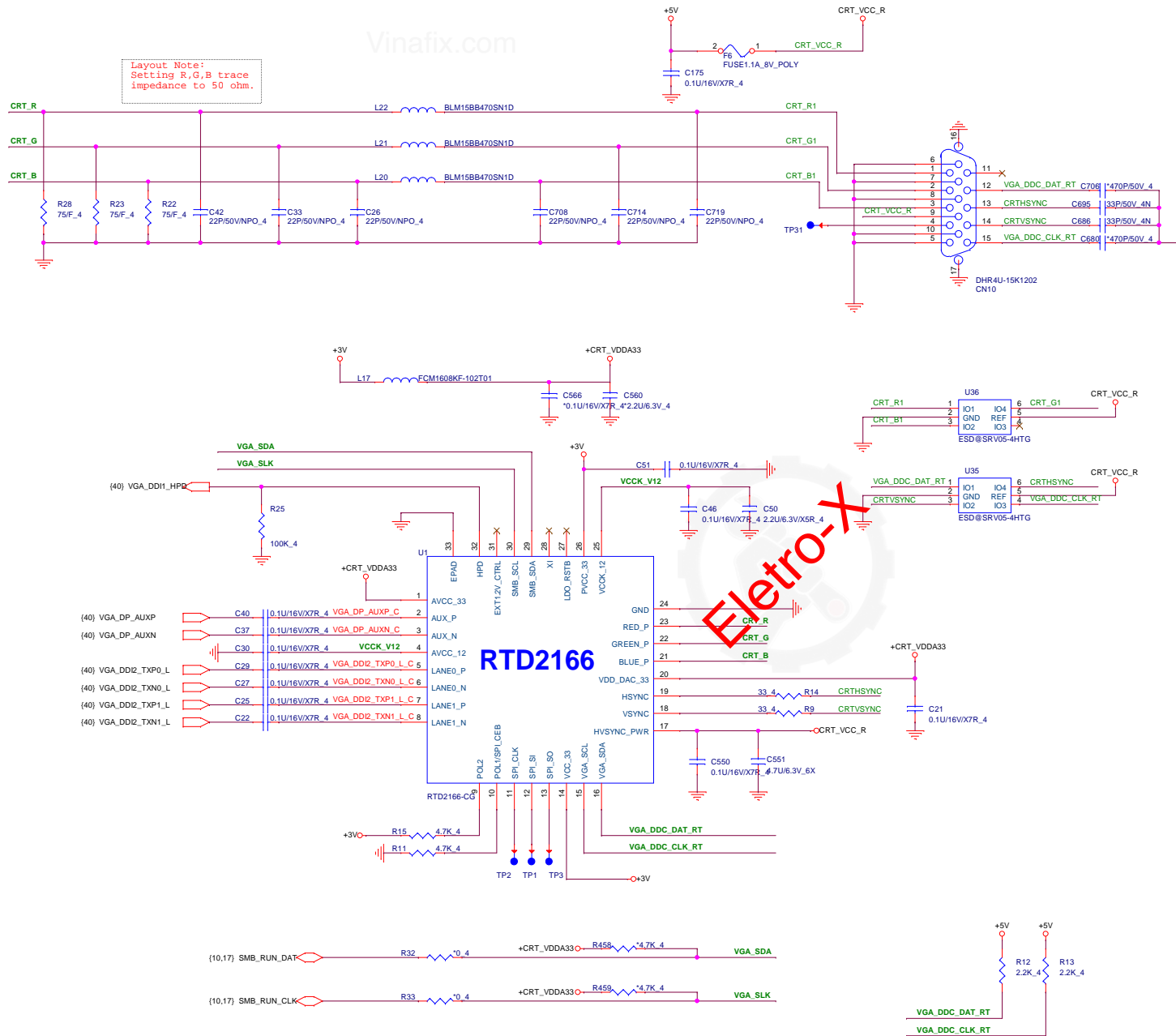


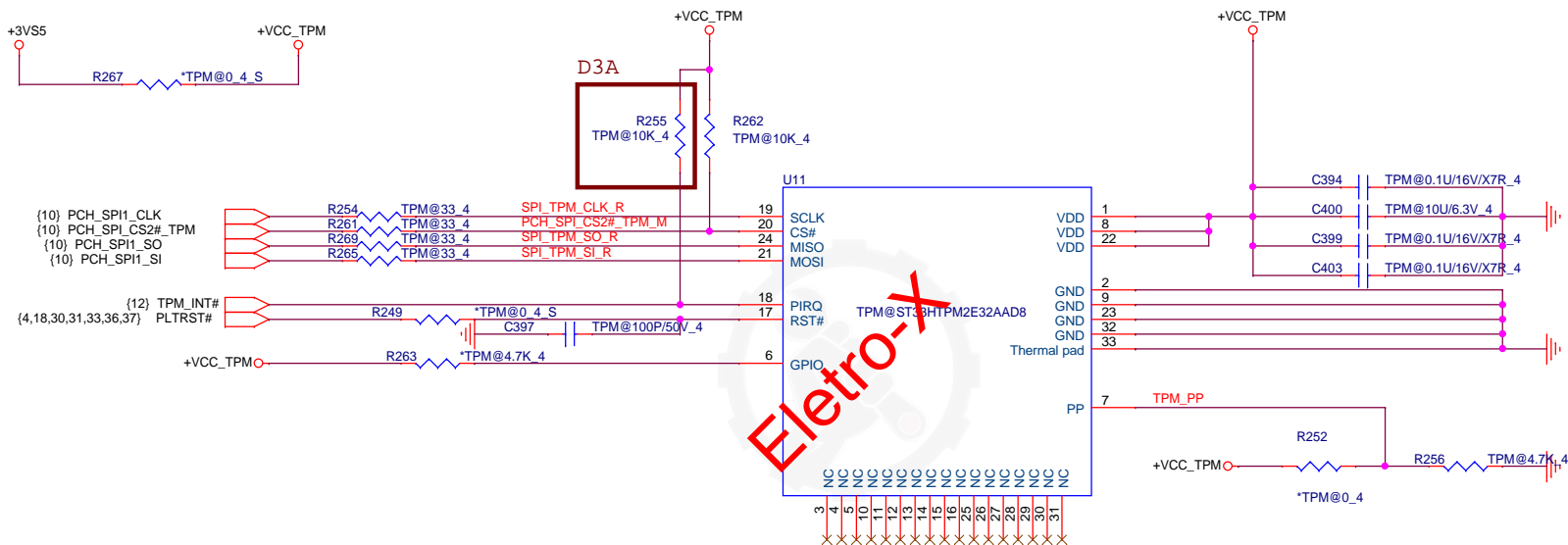
EMI reserve for HDMI

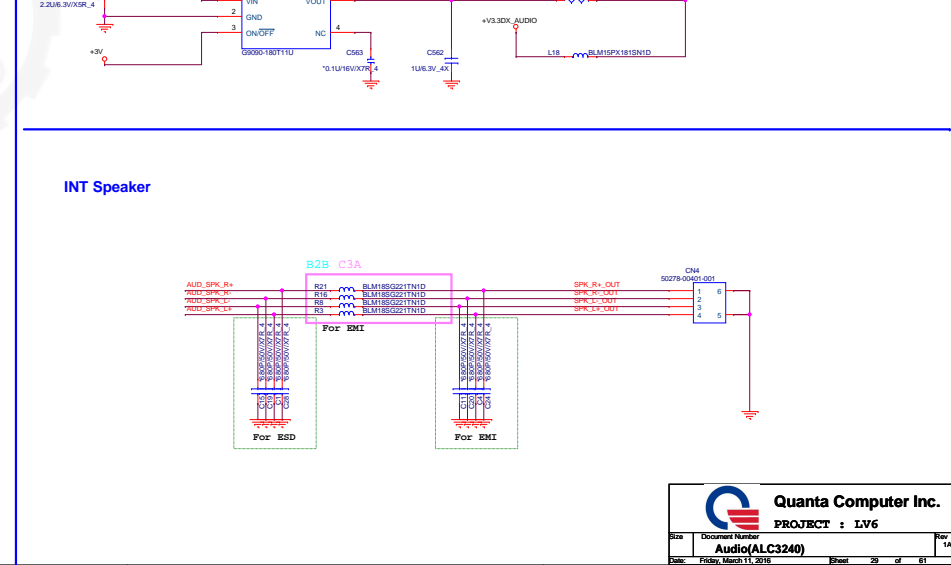
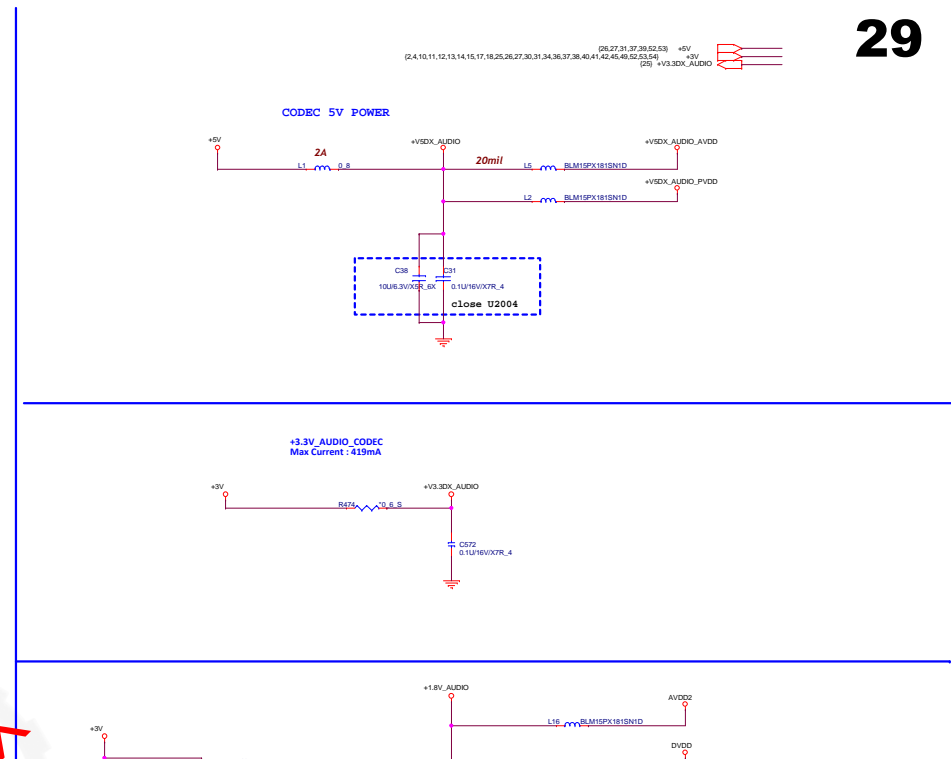


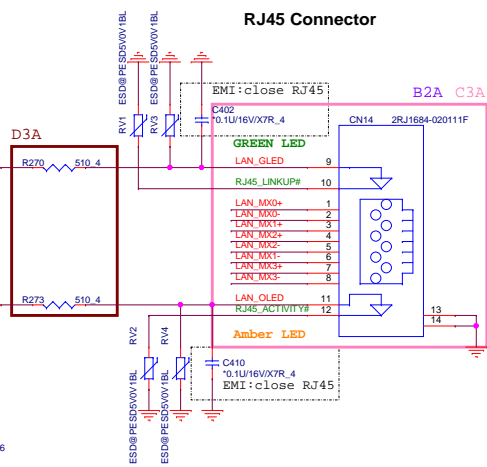
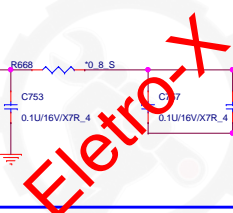
B2A



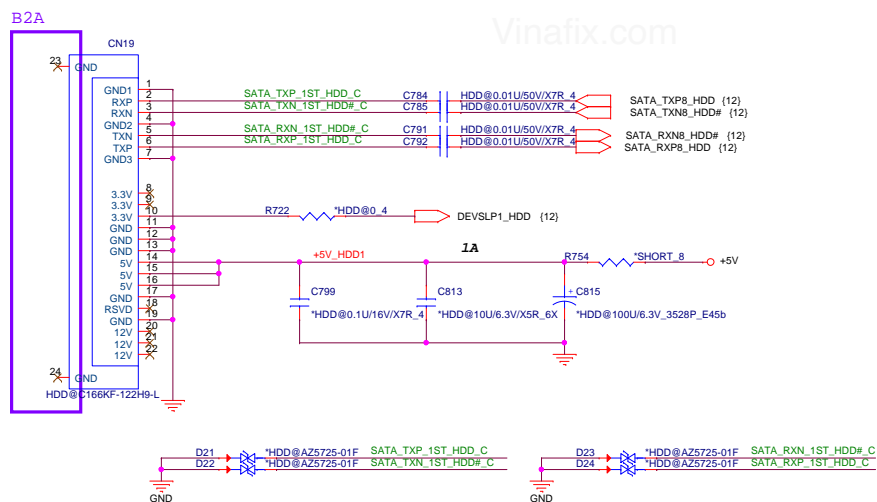




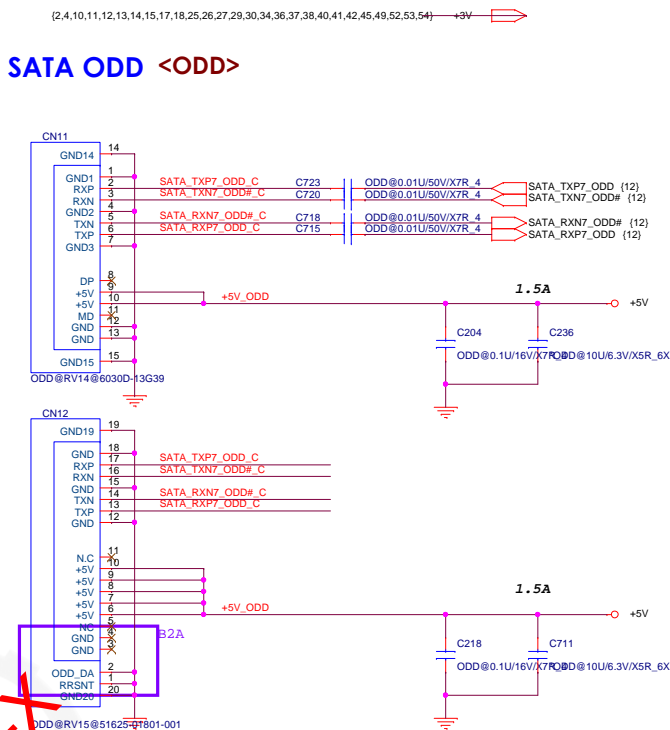




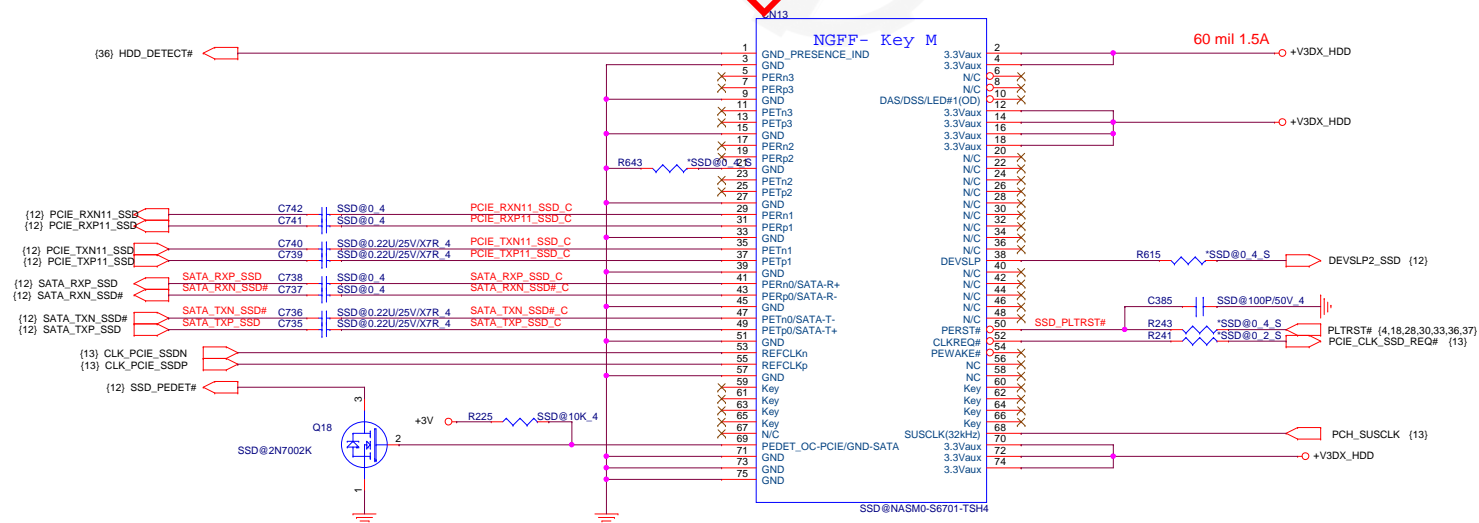
SATA HDD <HDD>



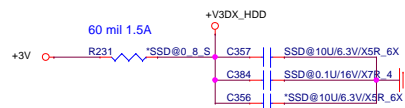
SATA ODD <ODD>



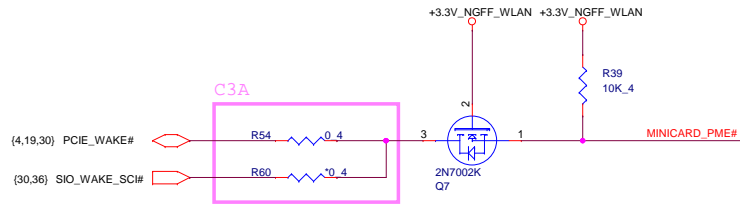
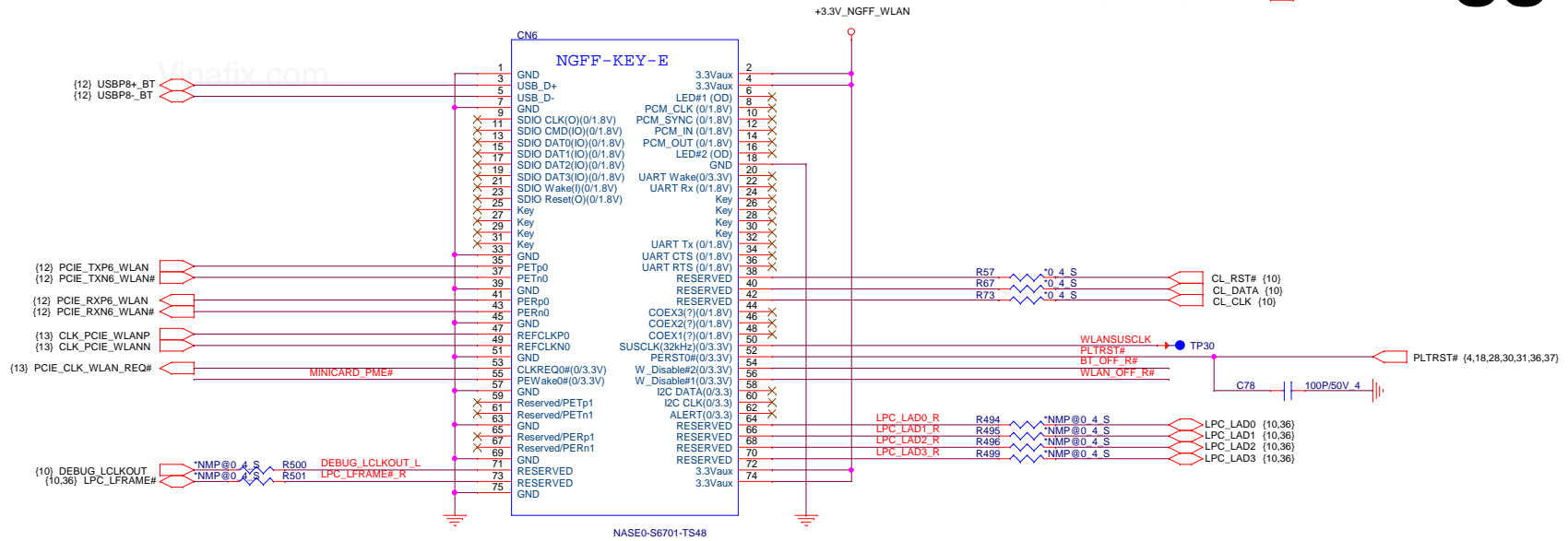
SSD M.2 <HDD>



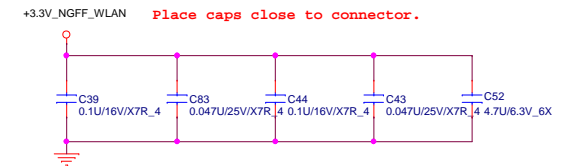
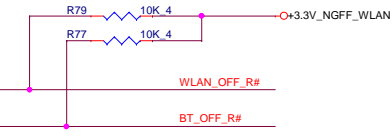
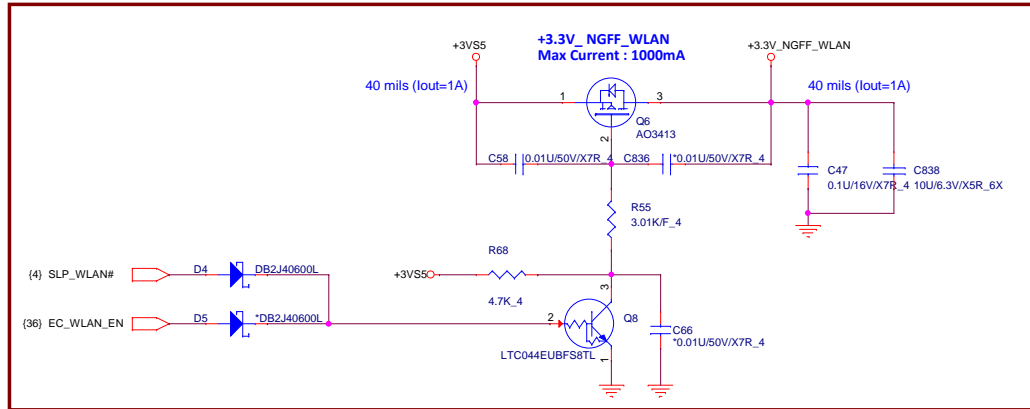
DC Current rating: 3 A (MAX)



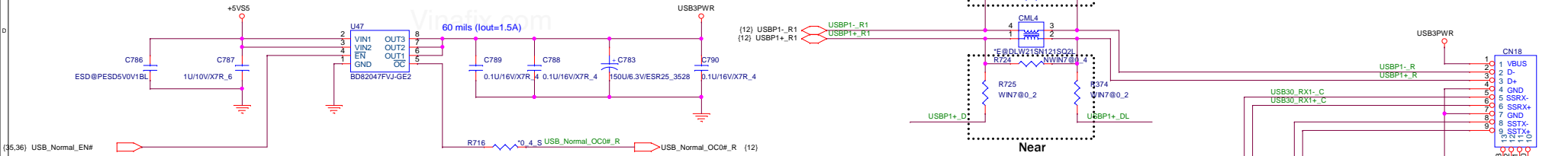




D3A



USB3.0 PORT0



LOW ACTIVE

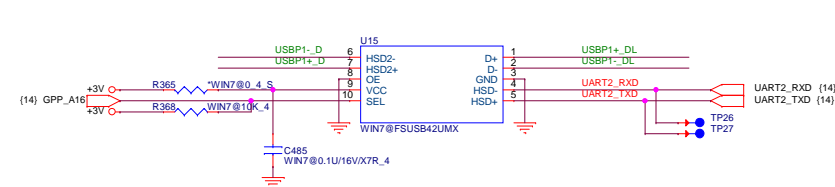
For ESD



For ESD

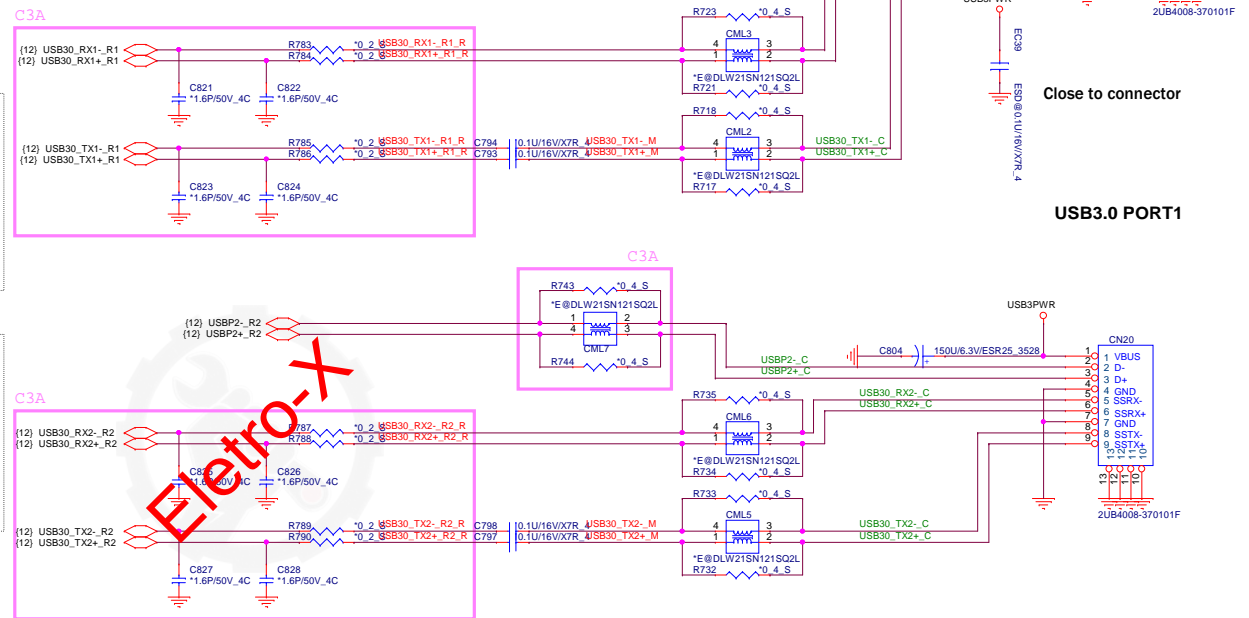


UART for DEBUG <W7D>



Close to connector

USB3.0 PORT1

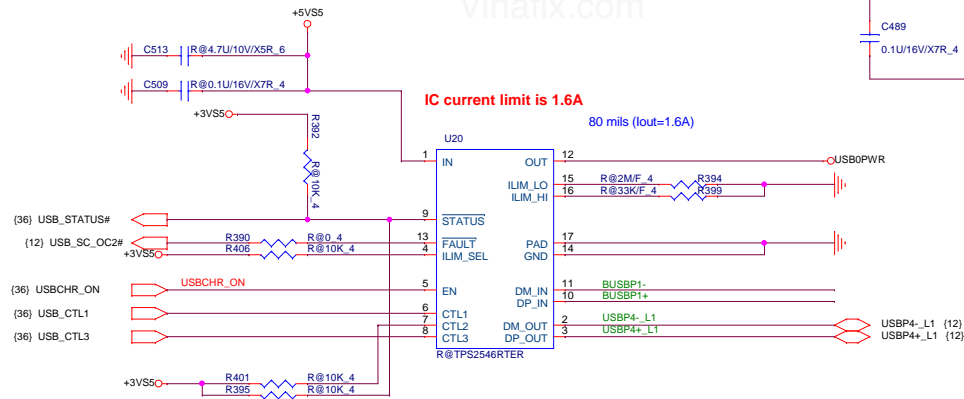


Close to connector

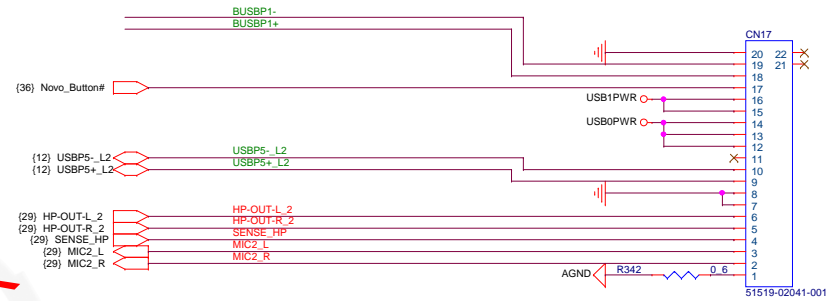
USB Sleep&Charger

<UBC> <UB2>

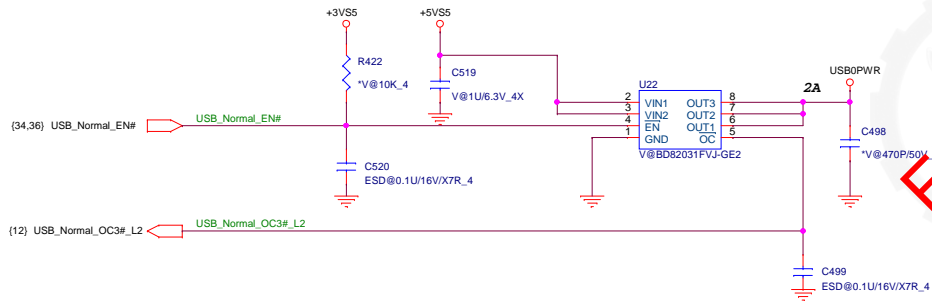
Vinafix.com



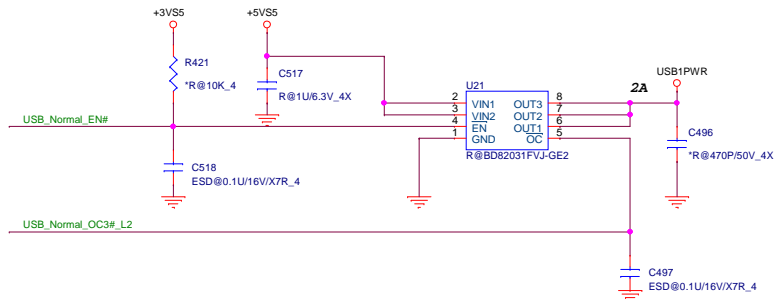
USB3.0 (with AOU5)

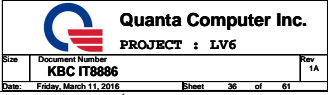


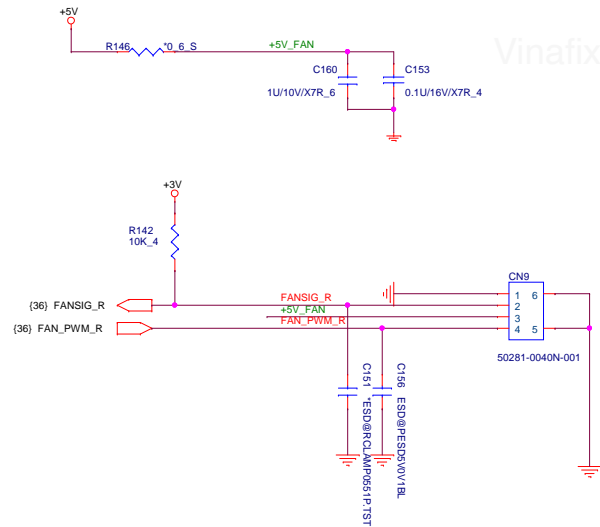
USB2.0 Power SW <UB2>



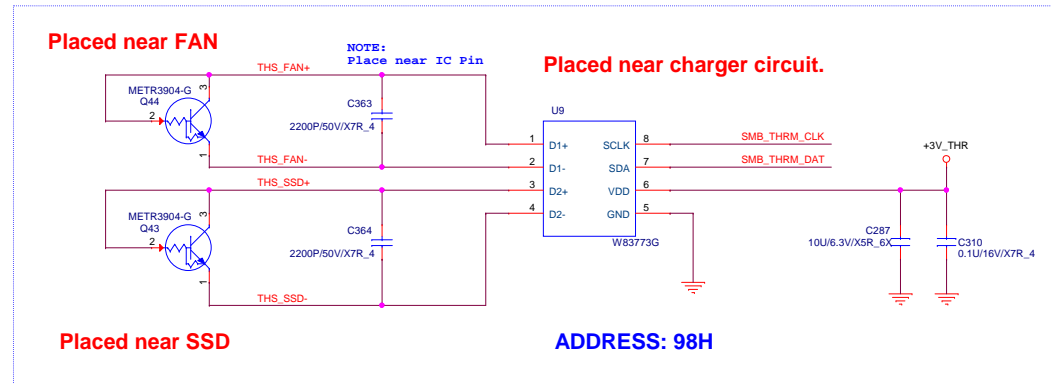
USB2.0 Power SW <UB2>



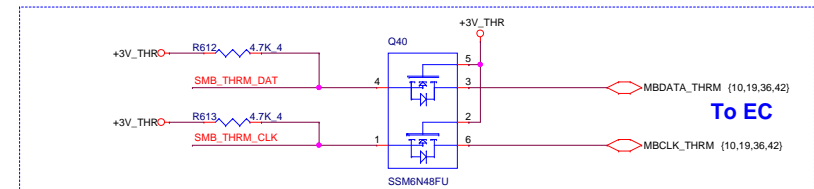
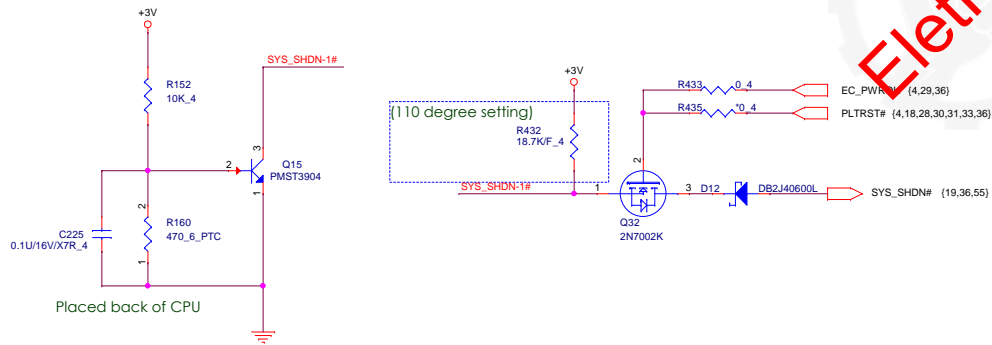




Thermal Sensor

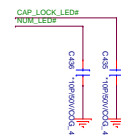
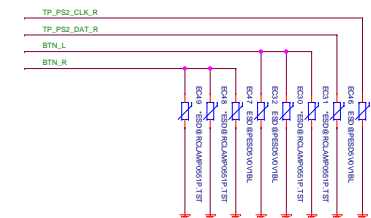


CPU PTC circuit

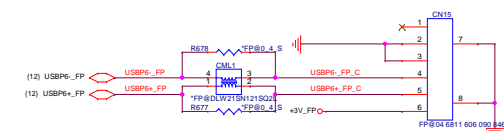
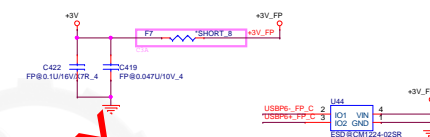


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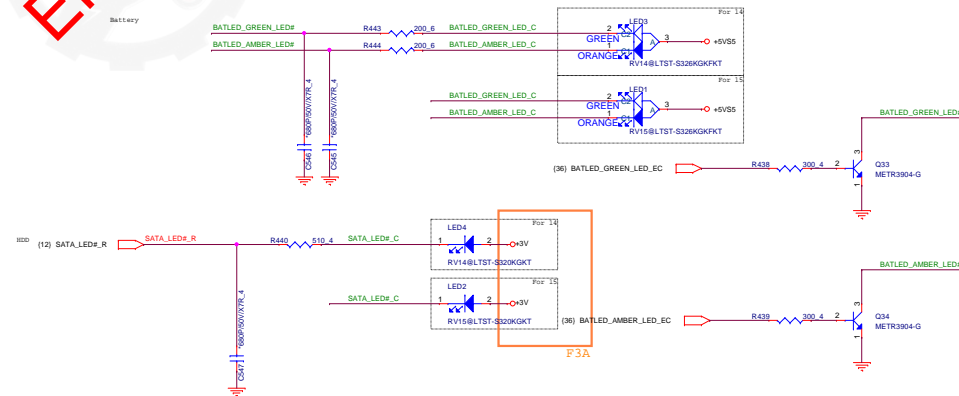
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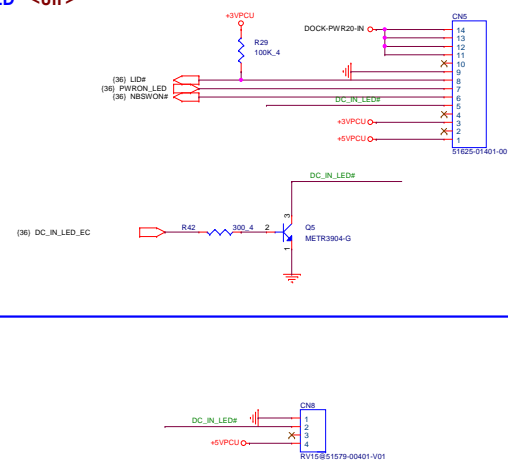
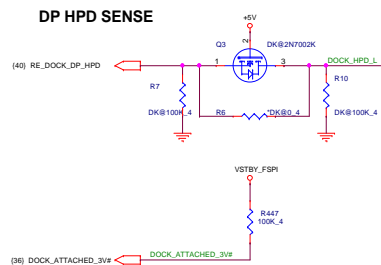
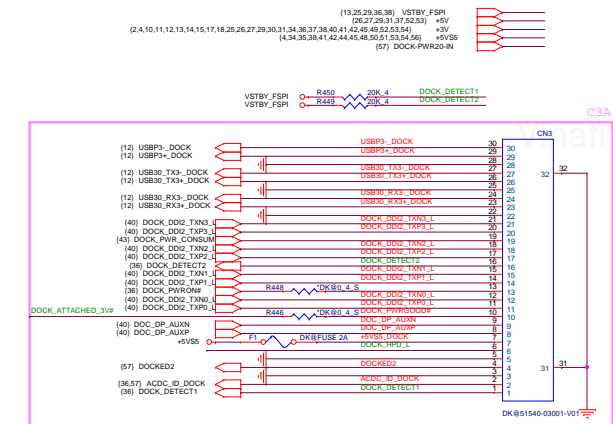


USB INTERFACE



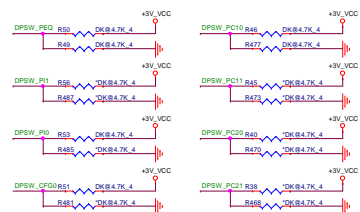
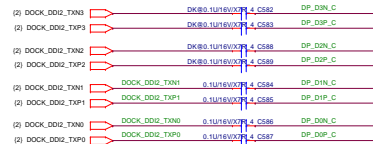
LED ~~<JIP>~~





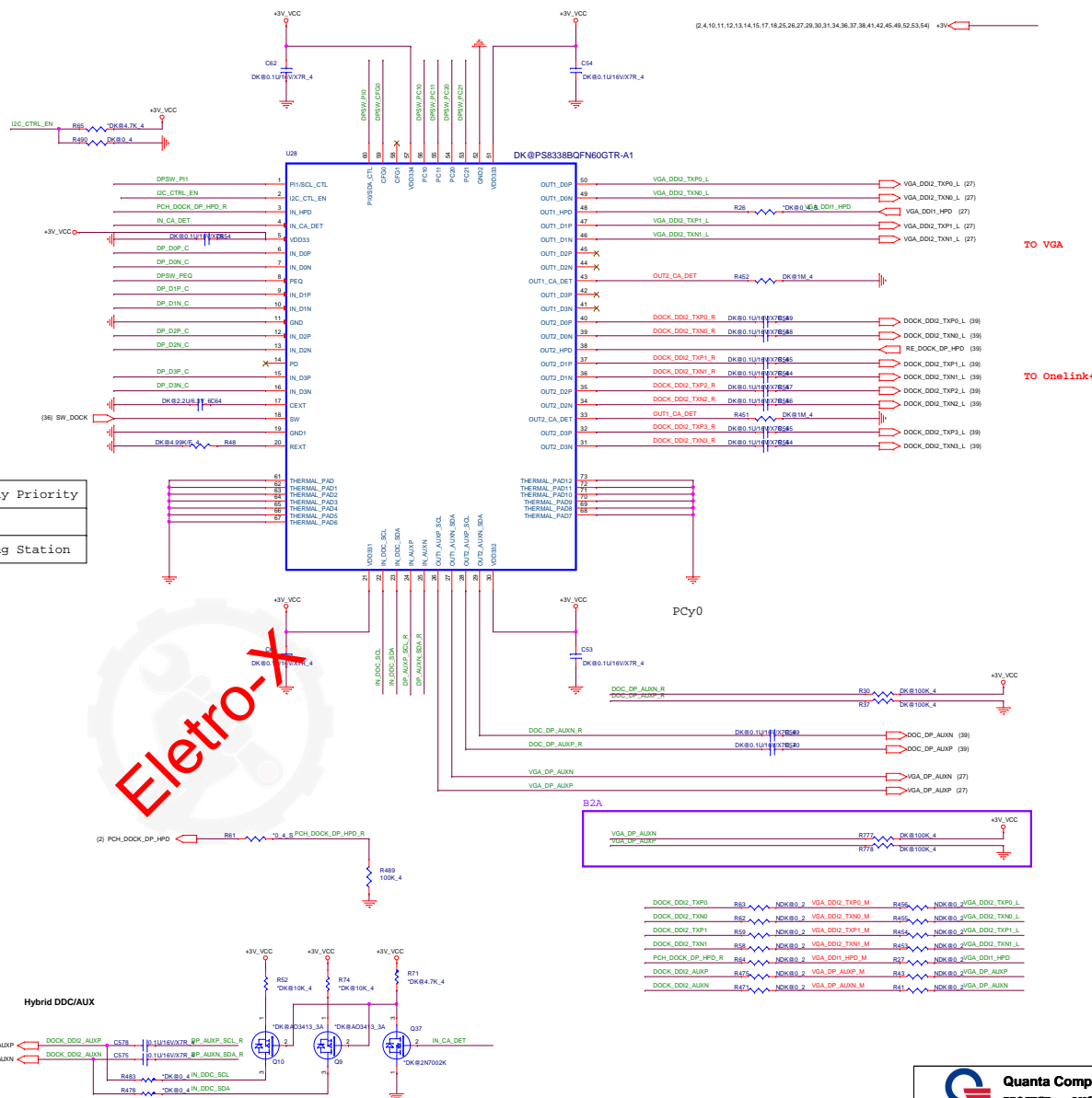


From CPU side

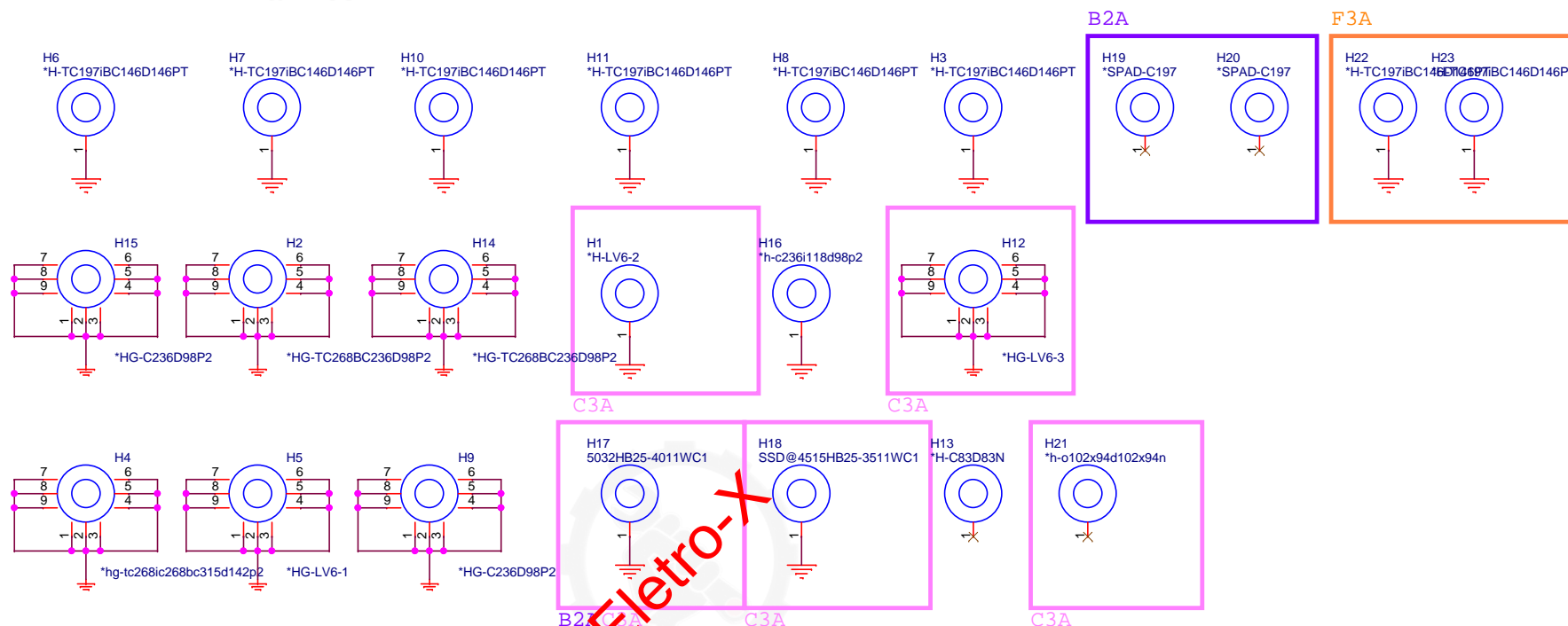


SW_DOCK	Display Priority
Low	VGA
High	Docking Station

PEQ	L	11.5dB (Default)
	H	14.5dB
	M	8.5dB
PI0	L	Automatic EQ enable (default)
	H	Automatic EQ disable
PI1	L	Auto test disable & input offset cancellation enable(default)
	H	Auto test enable & input offset cancellation enable
CFG0	L	Control Switching Mode (Default)
	H	Automatic Switching Mode
PCy0 (AUX Interception)	L	Link training (Default)
	H	800mV/ 0db
	M	400mV/ 0db
PCy1 (Swing)	L	Default
	H	+20%
	M	-16.7%

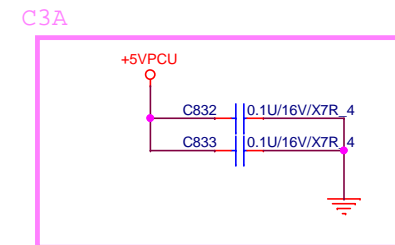
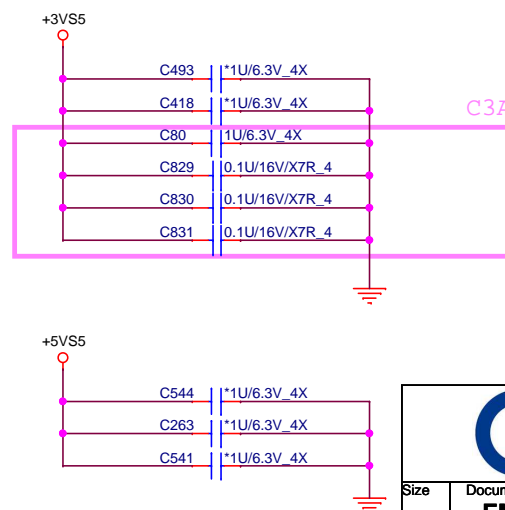
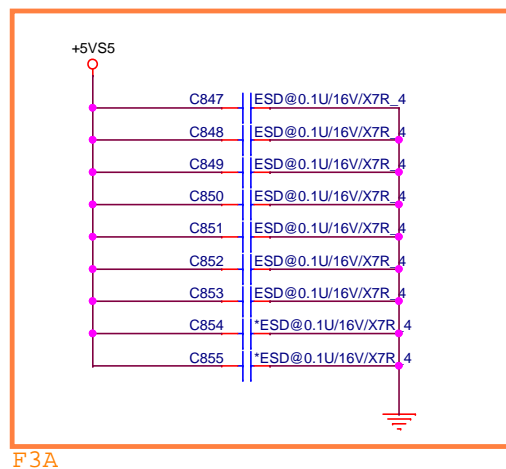
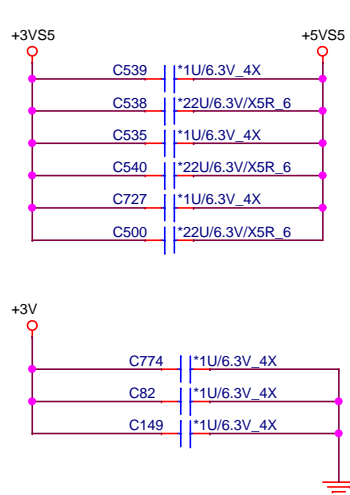


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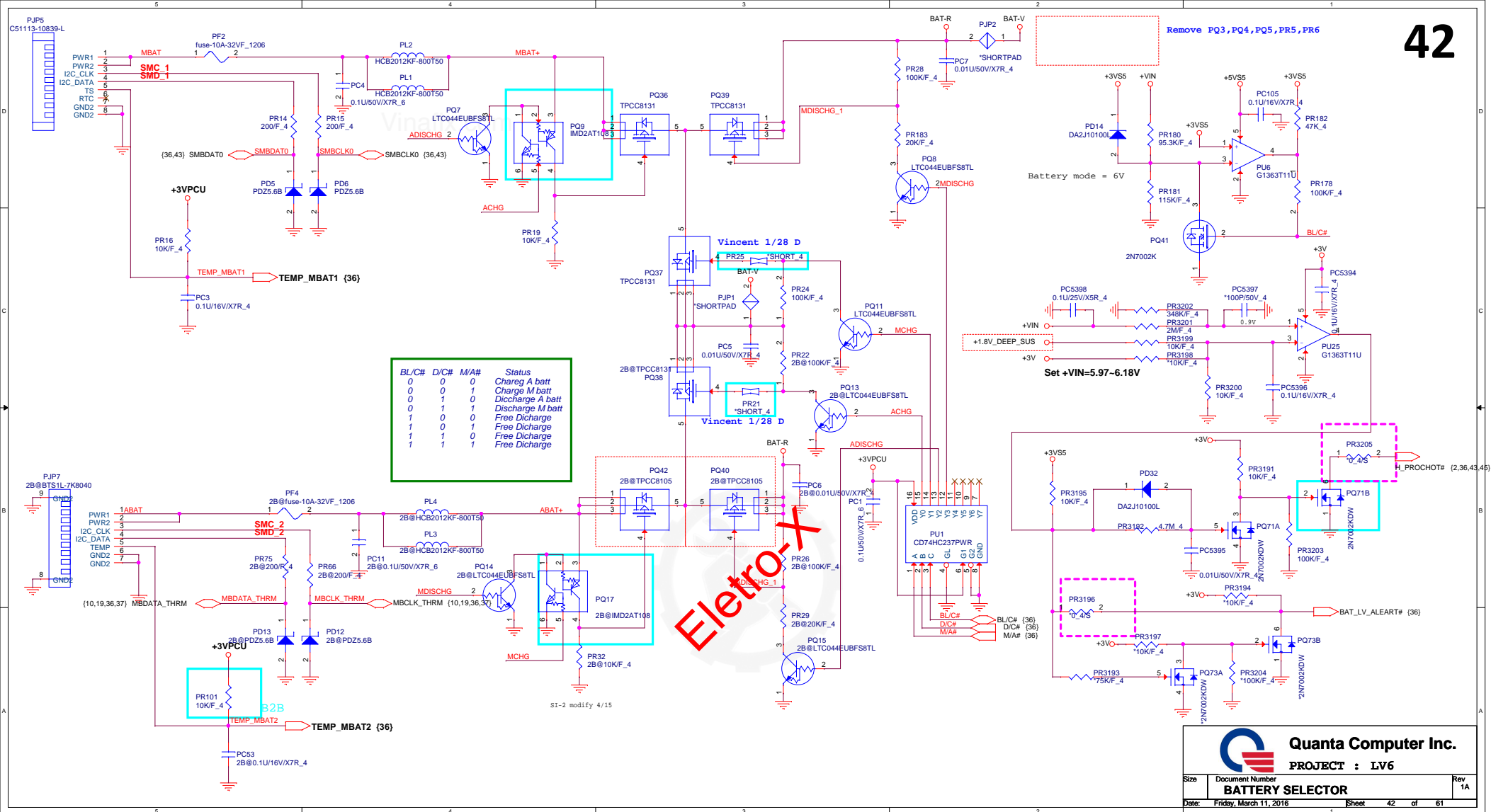


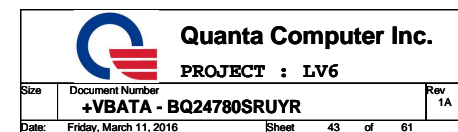
Eleto-X

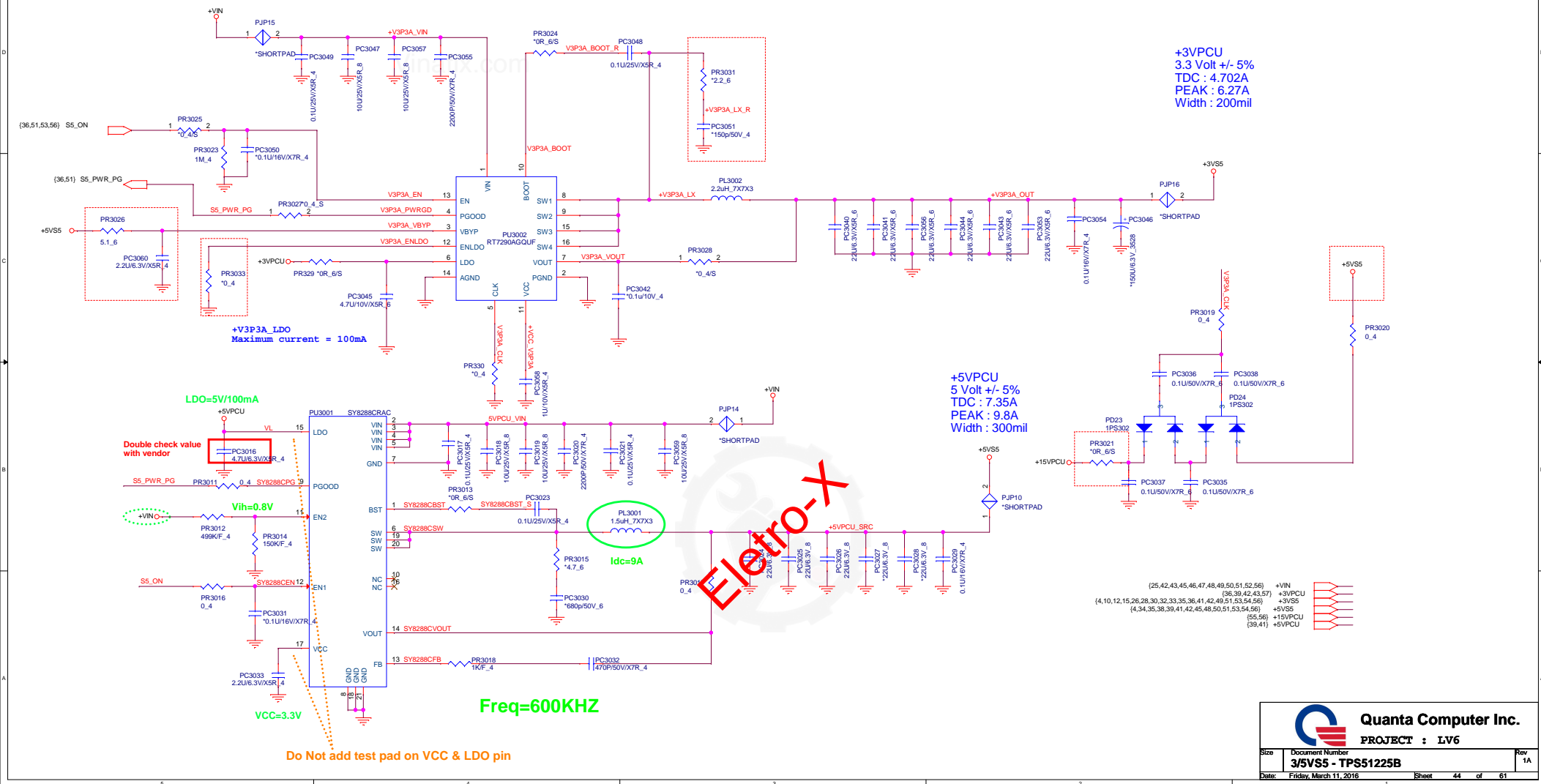
<EMC>



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	3/5VS5 - TPS51225B	1A
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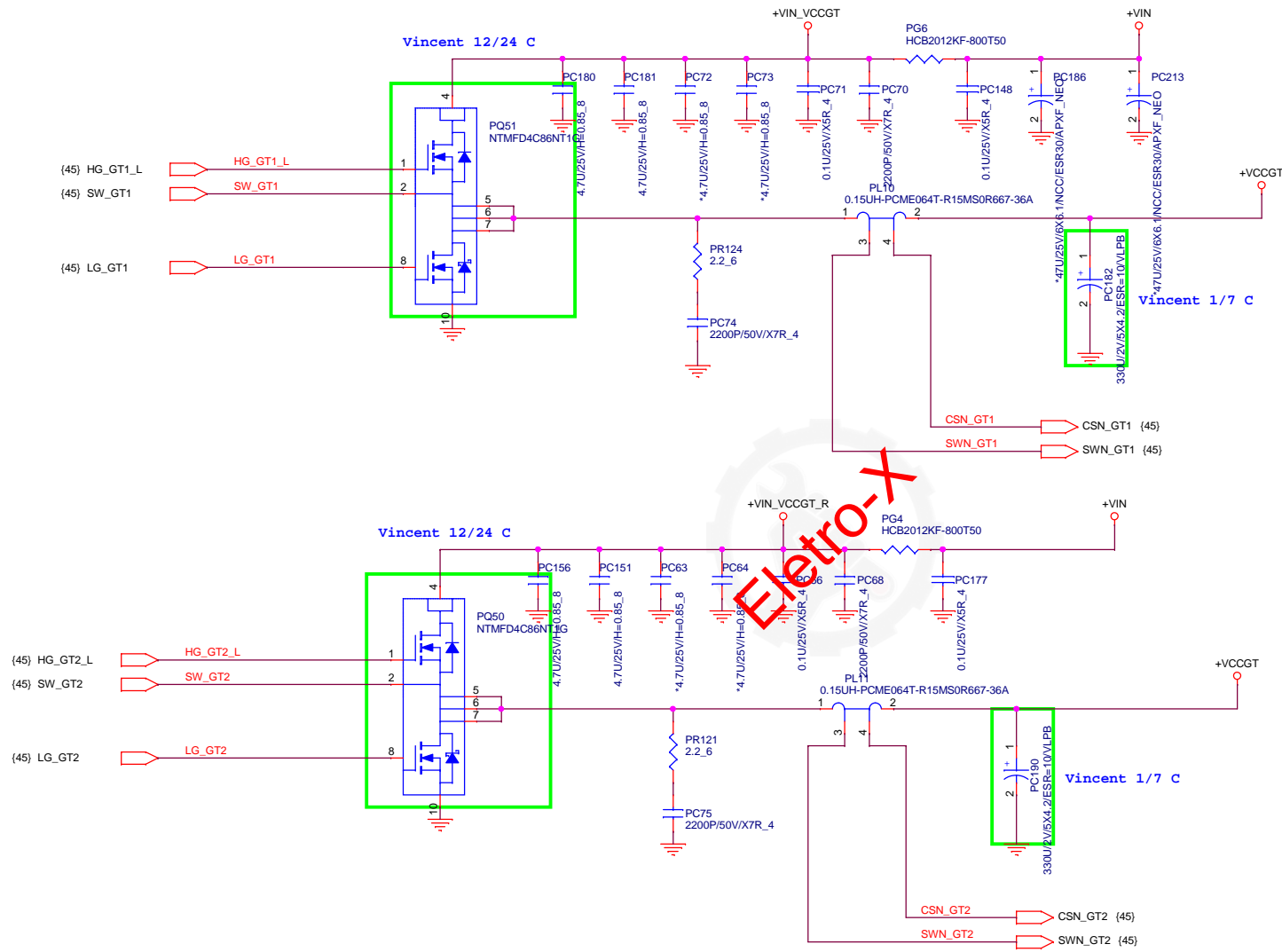



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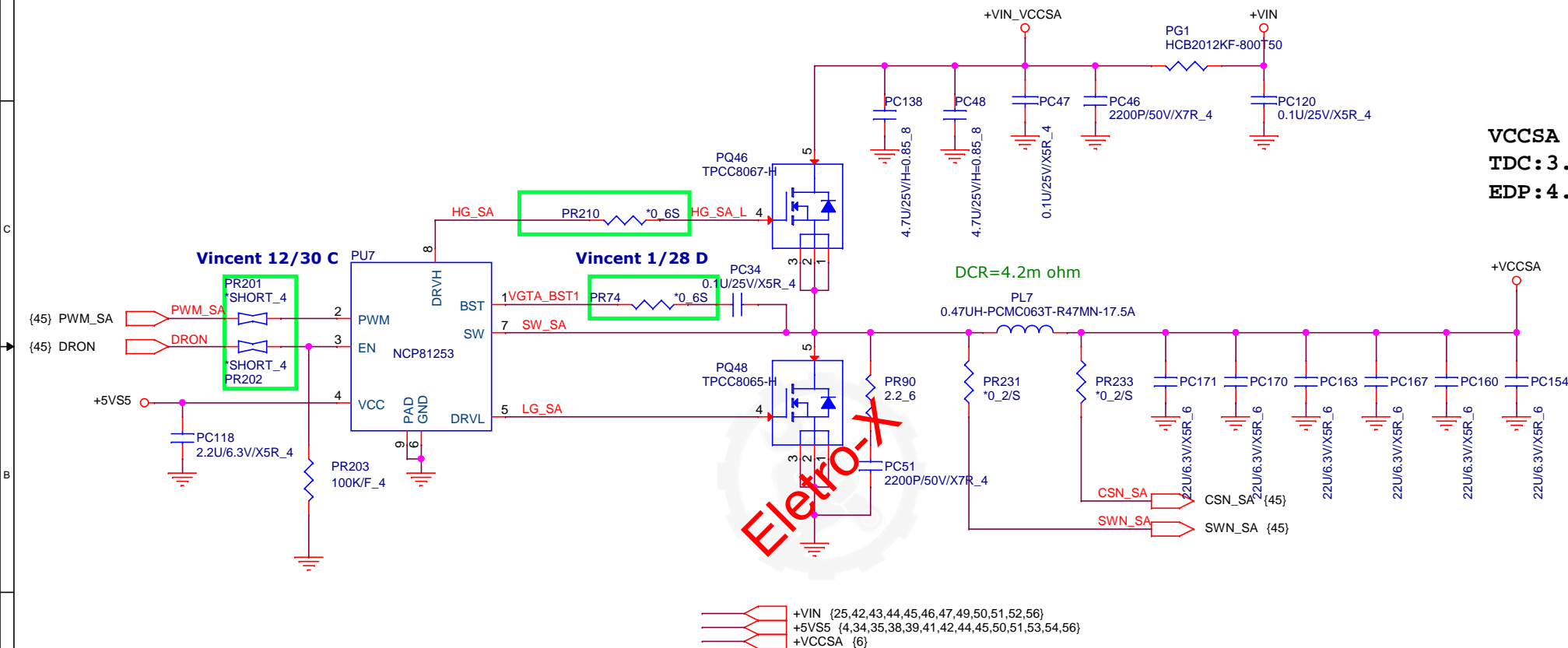
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Date:	Friday, March 11, 2016	Sheet 46 of 61

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+VCCGT
TDC :A
ICC_MAX :64A



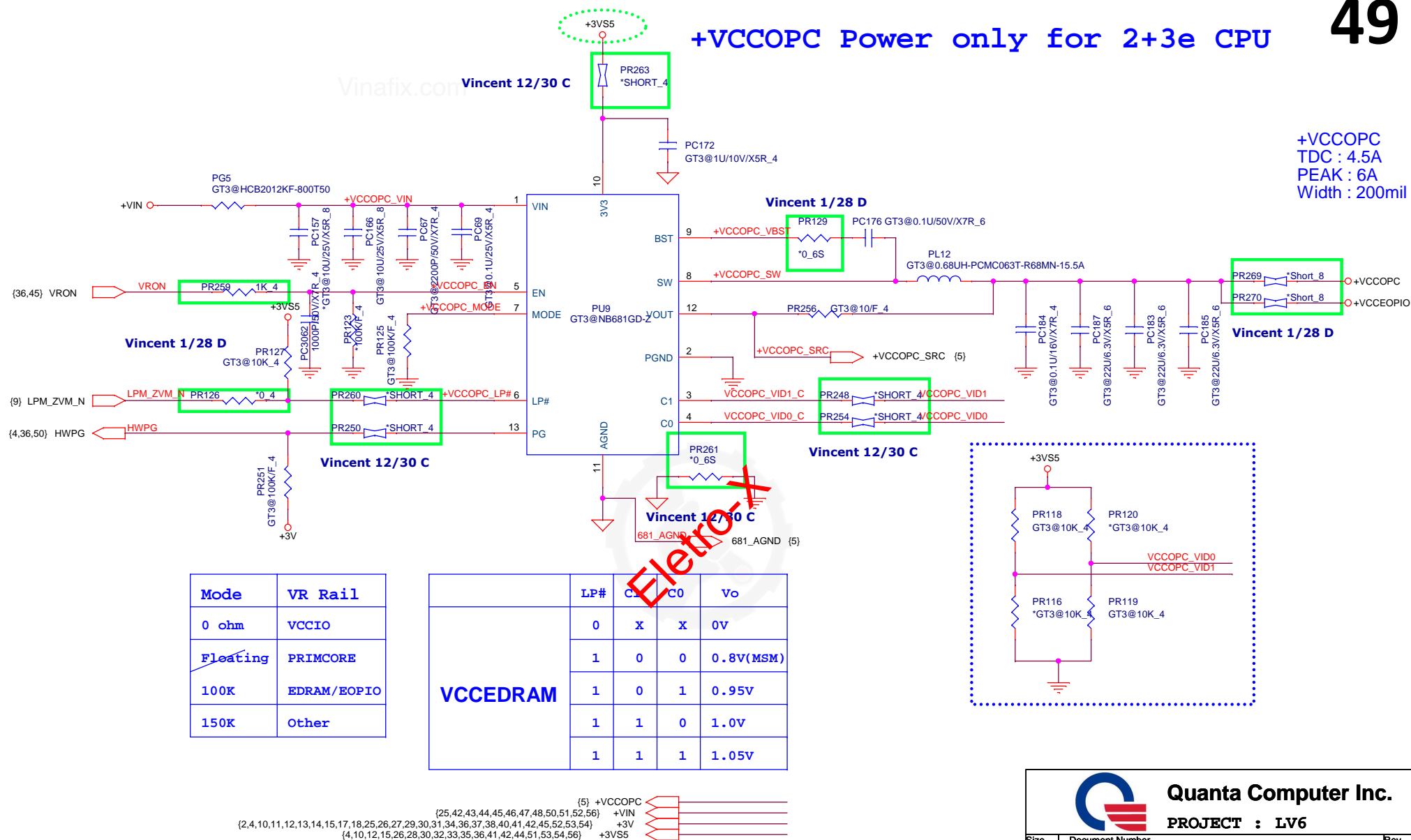
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		1A
Size	Document Number	
VCCGT		
Date:	Friday, March 11, 2016	Sheet 47 of 61



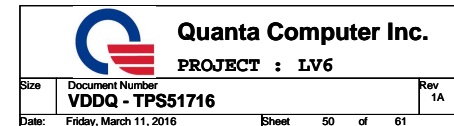
Quanta Computer Inc.

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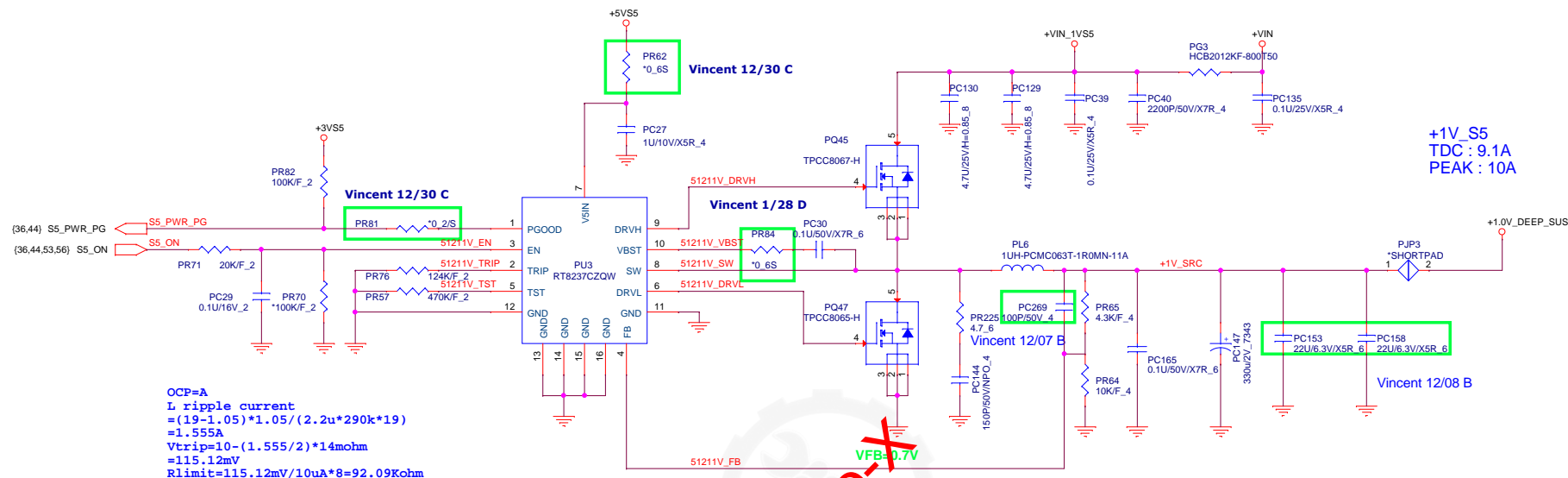
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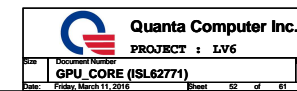


(25,42,43,44,45,46,47,48,49,51,52,56) +VIN
 (4,34,35,38,39,41,42,44,45,48,51,53,54,56) +5VS5
 {2,4,10,11,12,13,14,15,17,18,25,26,27,29,30,31,34,36,37,38,40,41,42,45,49,52,53,54} +3V
 {3,6,16,17} +1.2V_SUS
 {16,17} +0.6V_DDR_VTT

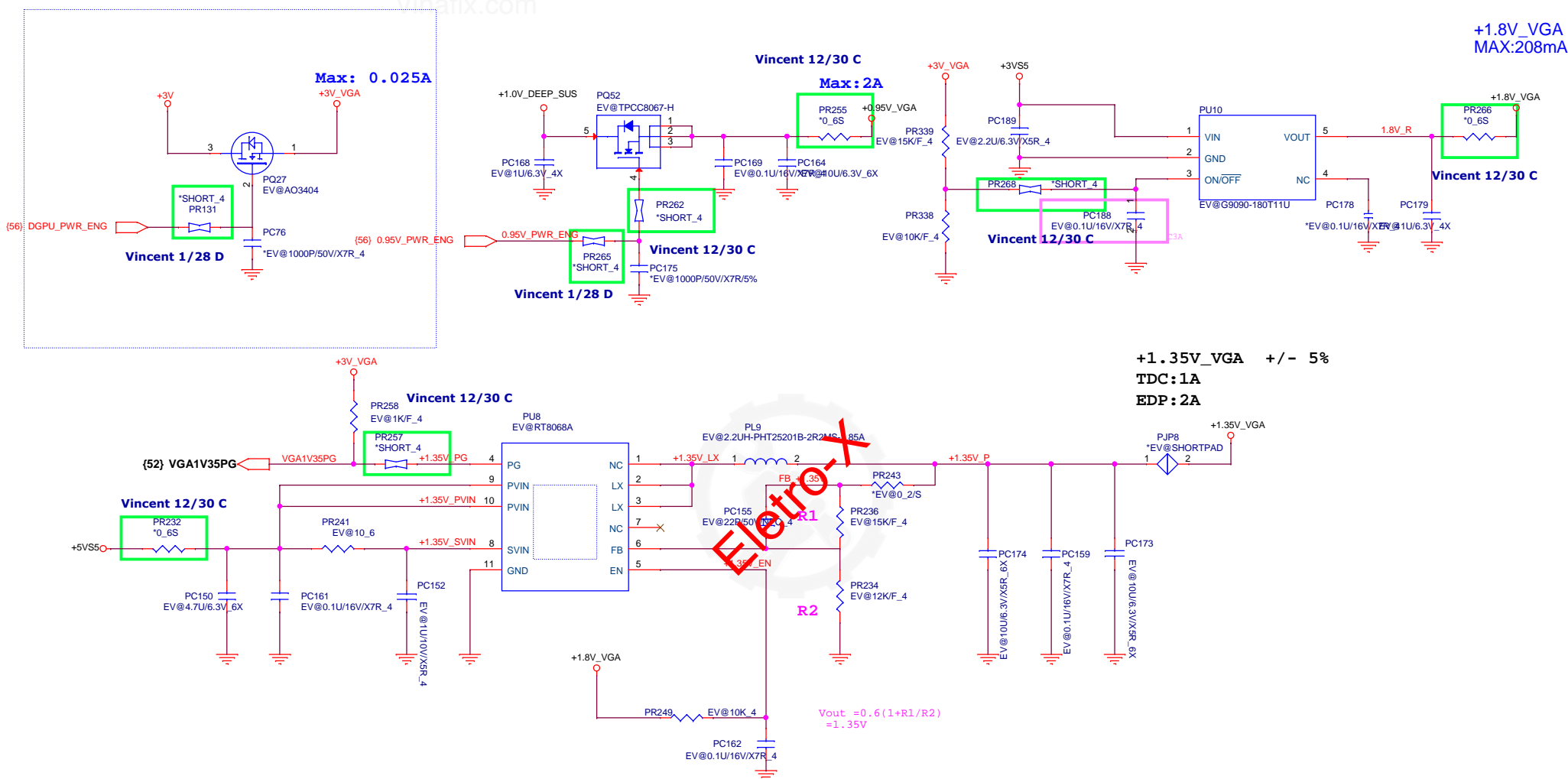


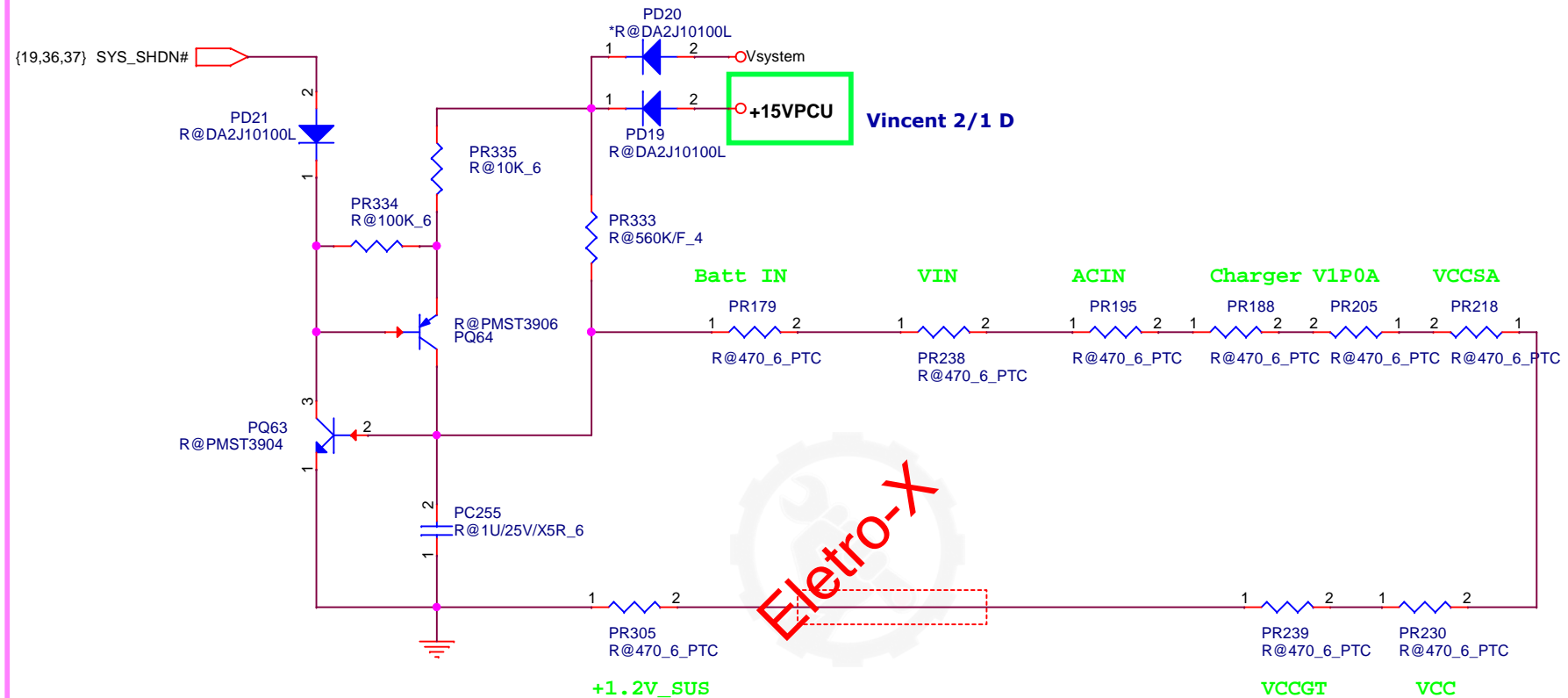
Vinafix.com





+1.8V_VGA(G9090-180T11U)
+1.35V_VGA(RT8068A)

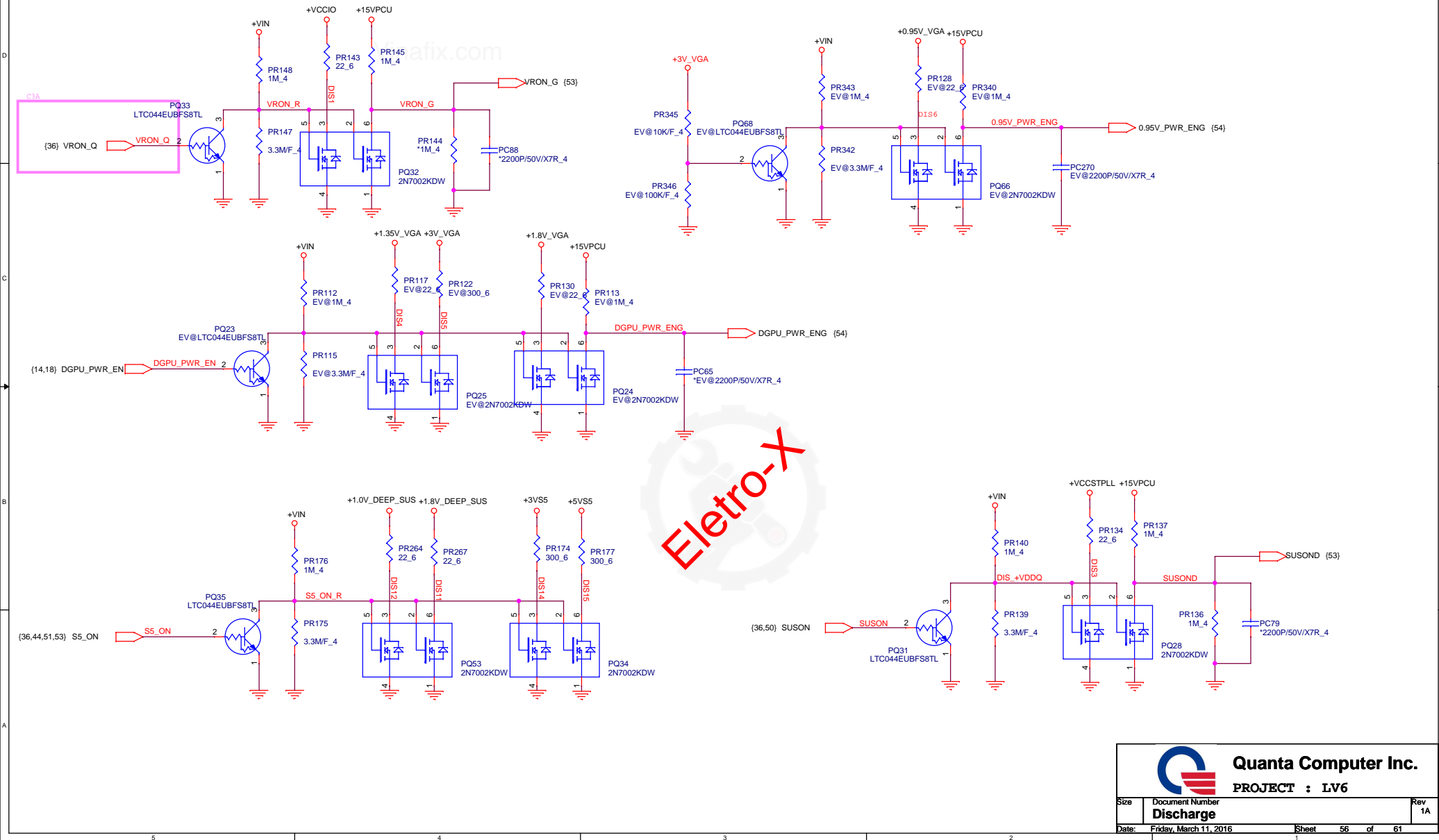


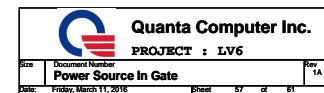


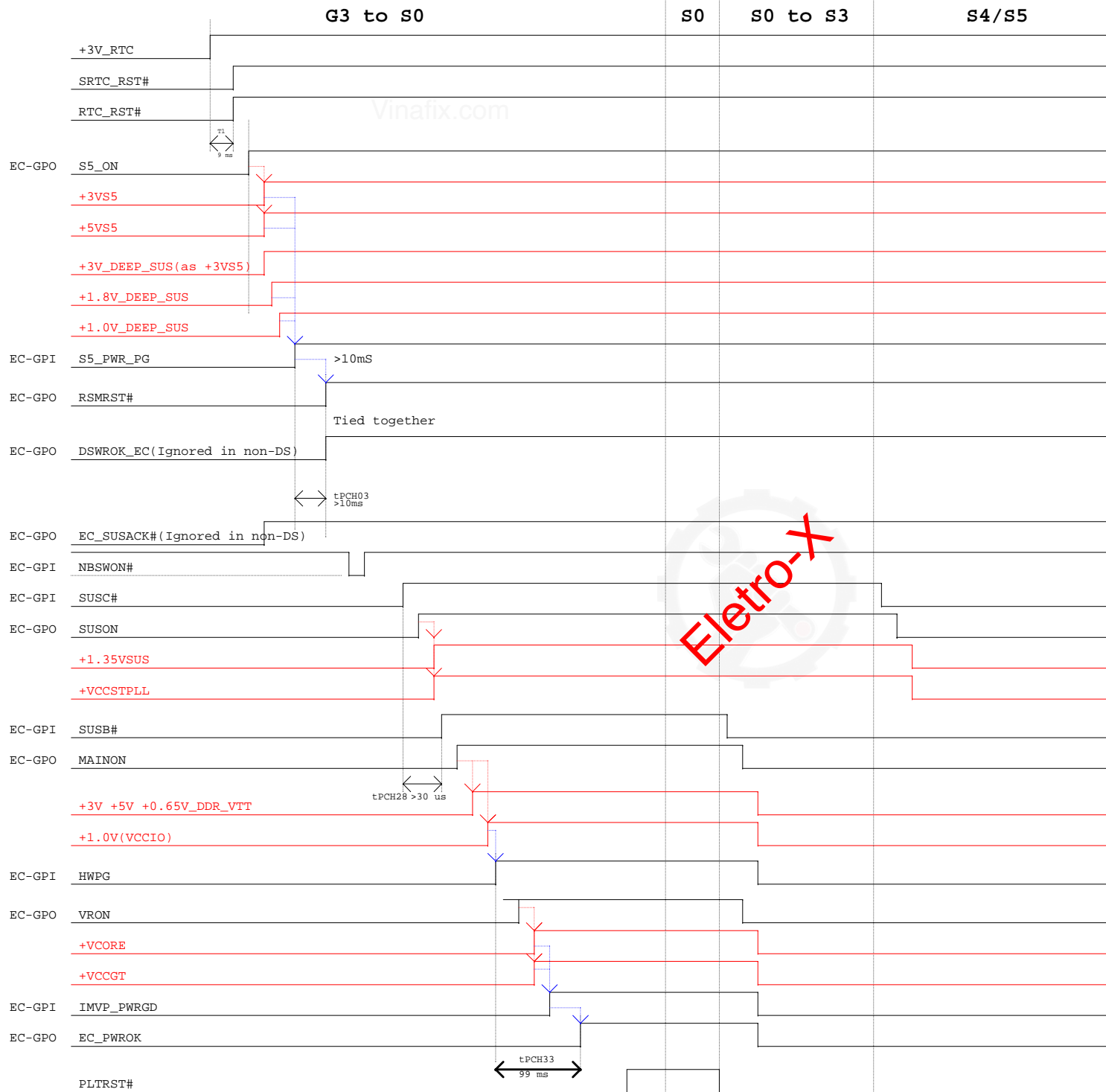
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2015	SDV-STAGE	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
		B2A	2	12/7	R780	Reserve PU 10K for
			4	12/7	R763	Add PU Res 10K for LAN_WAKE#.
			4	12/7	R764	Add PU Res 10K for VRALERT#.
			5	12/7	C819	Add Cap 1U for VCCSTG_G20.
			14	12/7	R768, R767	Add Board ID for SKYLAKE/ KABYLAKE.
			26	12/7	R769 、 R770 、 R771 、 R772 、 R773 、 R774 、 R775 、 R776	Add ohm for HDMI test
			30	12/7	CN14	Modify LAN connect pin define for LED
			31	12/7	CN19	Remove GND of stand pin for HDD connect
			31	12/7	CN12	Modify ODD connect to match FFC pin define
		B2B (R310)	30	12/18	CN14	Modify LAN connect pin define for LED
			4, 36	12/18	D10 、 R779 、 R780	Reserve DNBSWON# PU to +3VS5 and short 0 ohm
			13, 30	12/25	C755 、 C763 、 C359 、 C360	RTC CAP tuning
			29	12/25	R21 、 R16 、 R3 、 R8	FOR EMI

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